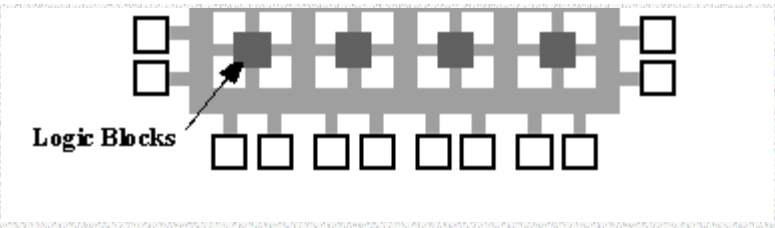

Fig. 2 The FPGA

The FPGA has three major configurable elements: configurable logic blocks (CLBs), input/outp blocks, and interconnects. The CLBs provide the functional elements for constructing user's log (**Figure 2**). The IOBs provide the interface between the package pins and internal signal lines. T programmable interconnect resources provide routing paths to connect the inputs and outputs o the CLBs and IOBs onto the appropriate networks. Customized configuration is established by programming internal static memory cells that determine the logic functions and internal connections implemented in the FPGA.

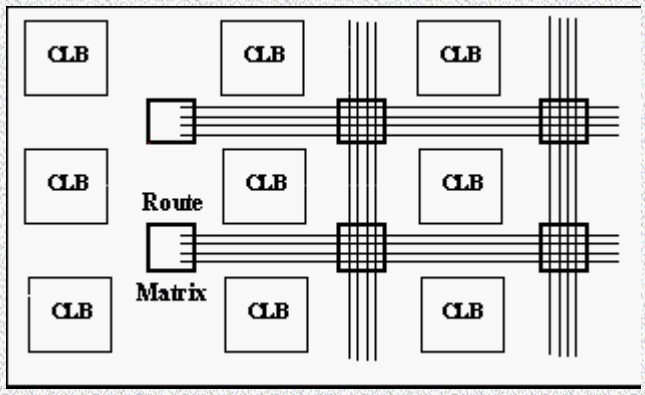

Fig. 3 CLBs Interconnects

Figure 3 depicts a FPGA with a two-dimensional array of logic blocks that can be interconnect by interconnect wires. All internal connections are composed of metal segments with programmable switching points to implement the desired routing. An abundance of different routing resources is provided to acheive efficient automated routing. There are four main types interconnect, three are distinguished by the relative length of their segments: single-length lines double-length lines and Longlines. (NOTE: The number of routing channels shown in the figur are for illustration purposes only; the actual number of routing channels varies with the array si In addition, eight global buffers drive fast, low-skew nets most often used for clocks or global control signals.