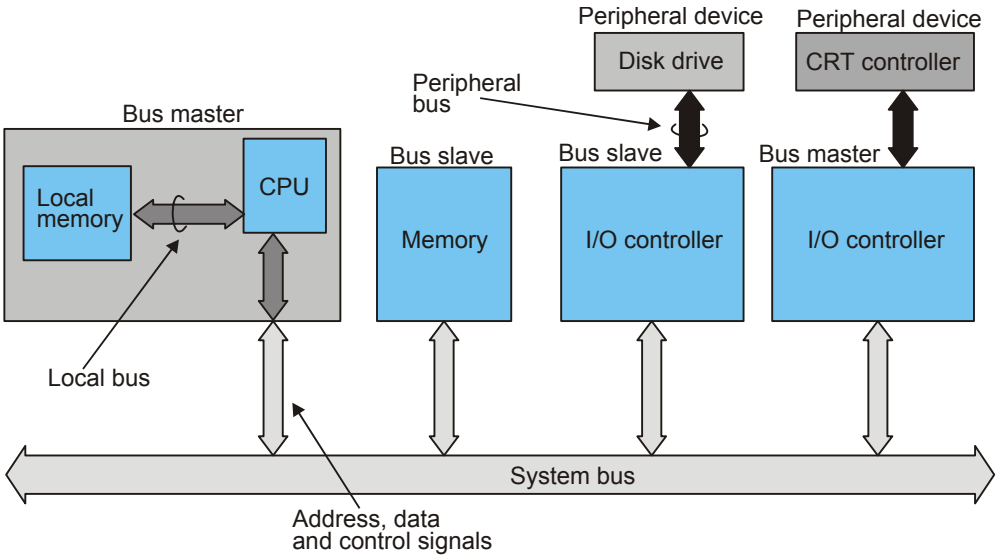
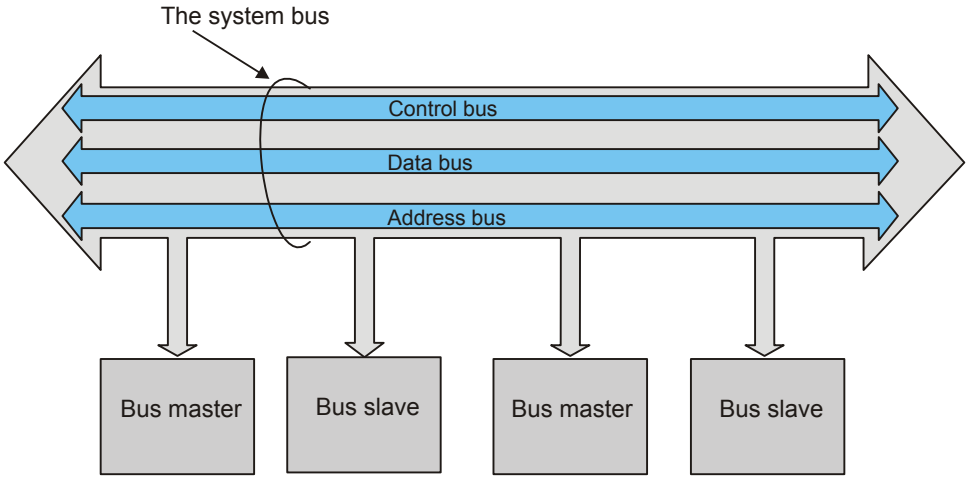
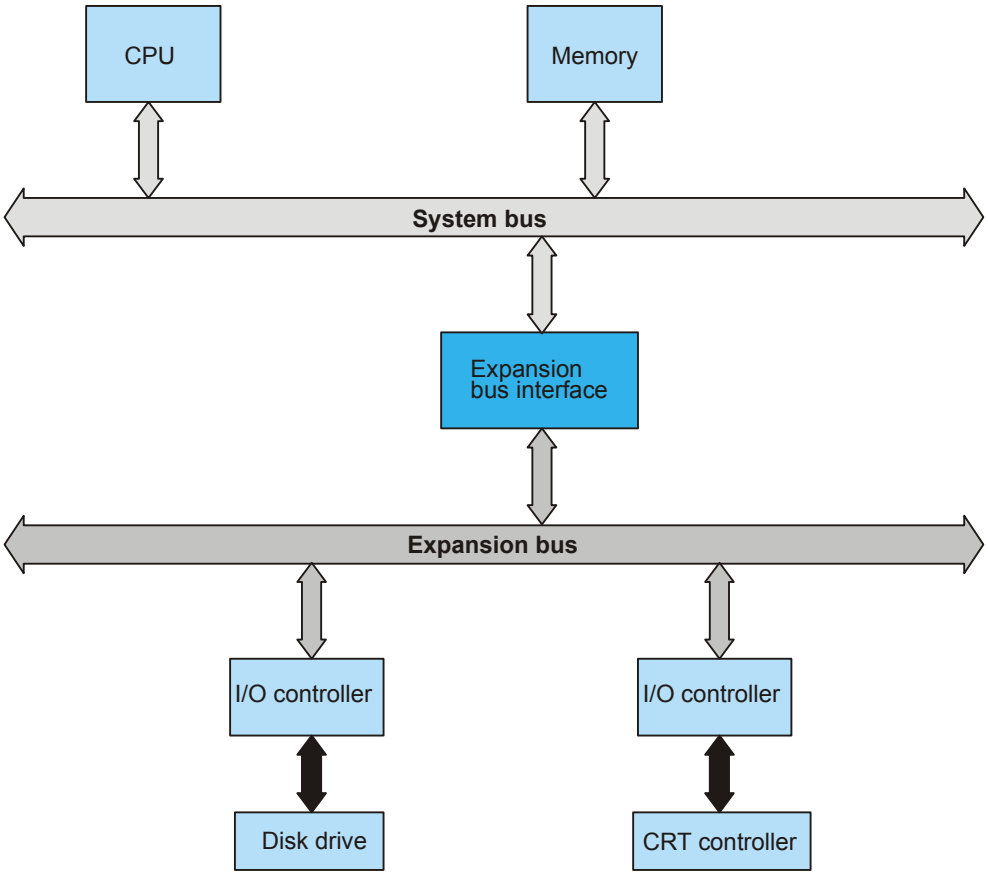
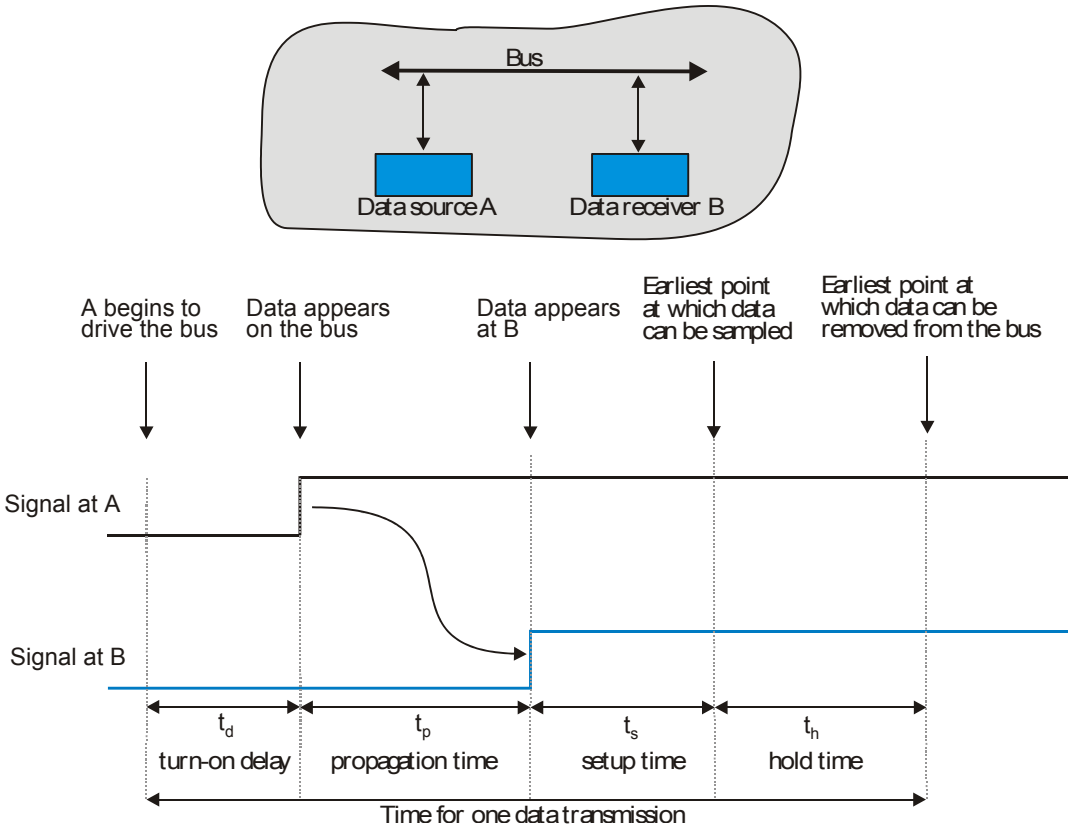
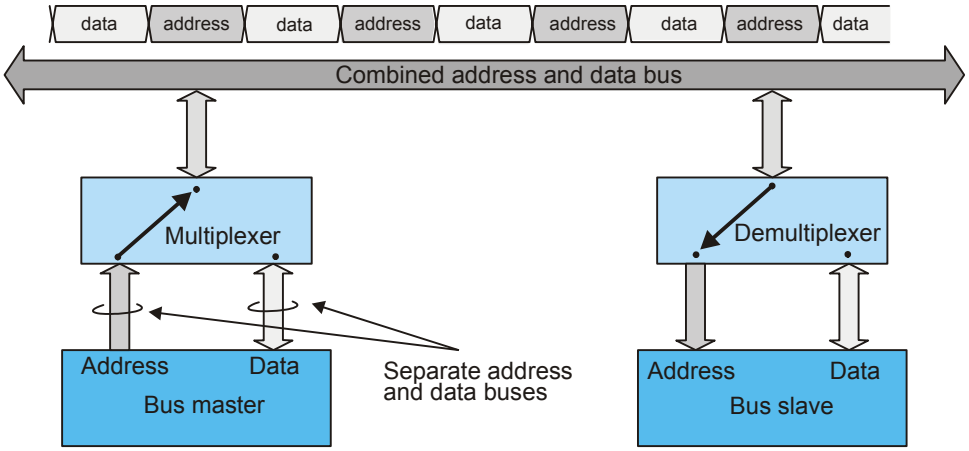
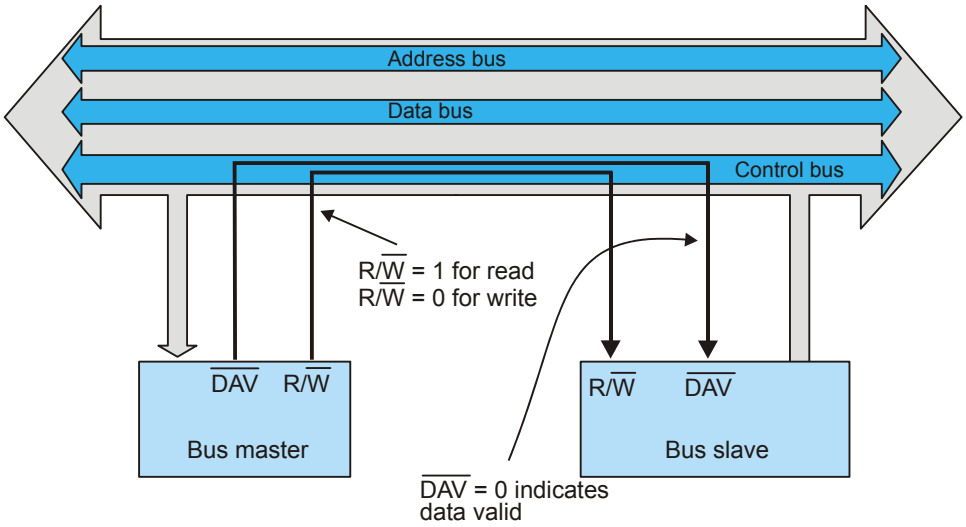

Peripheral device
Disk drive
Peripheral device
CRT controller
Peripheral
bus
Bus master
Local
memory
CPU
Bus slave
Memory
Bus slave
I/O controller
Bus master
I/O controller
Local bus
System bus
Address, data
and control signals

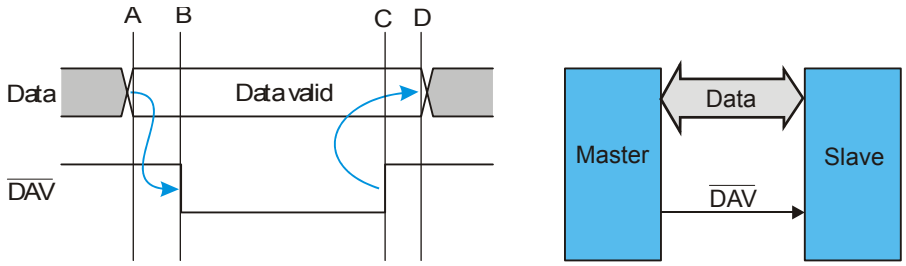

The system bus
Control bus
Data bus
Address bus
Bus master
Bus slave
Bus master
Bus slave

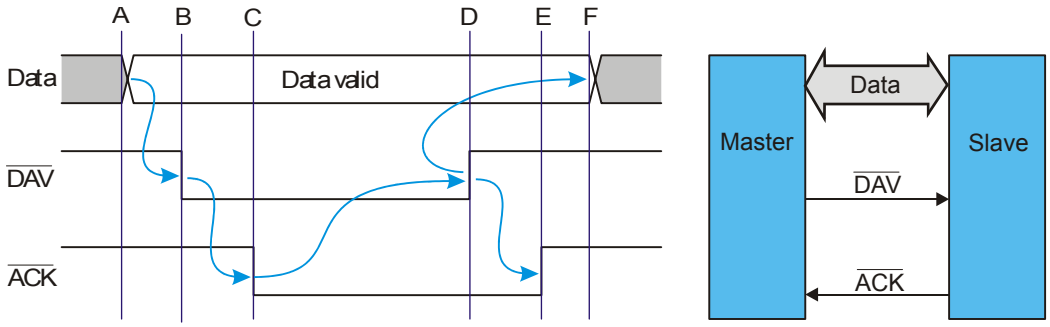

CPU
Memory
System bus
Expansion
bus interface
Expansion bus
I/O controller
I/O controller
Disk drive
CRT controller

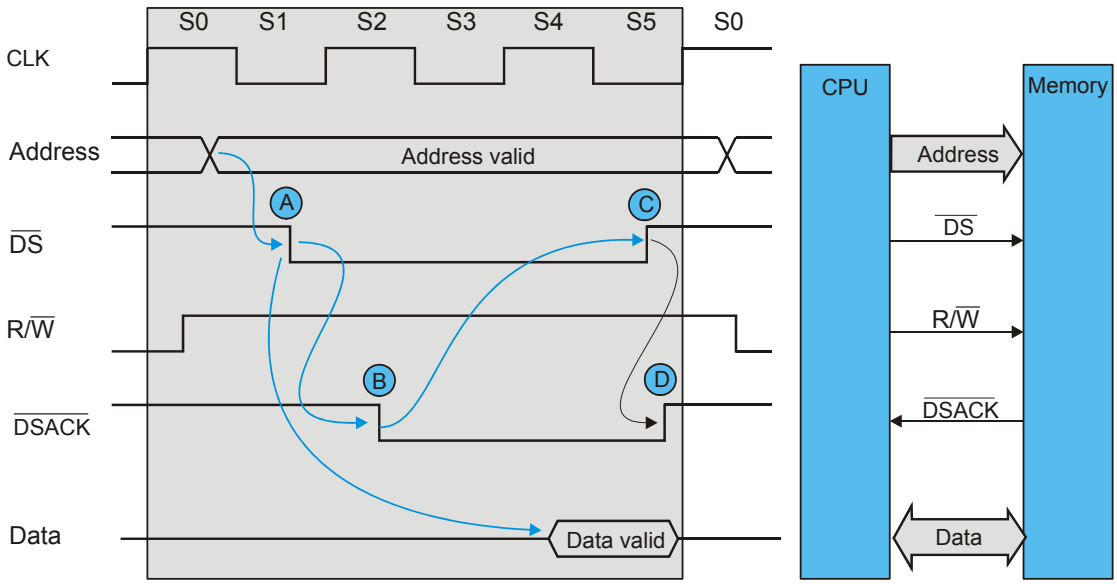

Bus
Data source A
Data receiver B
A begins to drive the bus
Data appears on the bus
Data appears at B
Earliest point at which data can be sampled
Earliest point at which data can be removed from the bus
Signal at A
Signal at B
t_d
turn-on delay
t_p
propagation time
t_s
setup time
t_h
hold time
Time for one data transmission


data
address
data
address
data
address
data
address
data
Combined address and data bus
Multiplexer
Demultiplexer
Address
Data
Bus master
Separate address
and data buses
Address
Data
Bus slave


Address bus
Data bus
Control bus
R/$\overline{W}$ = 1 for read
R/$\overline{W}$ = 0 for write
$\overline{DAV}$
R/$\overline{W}$
Bus master
R/$\overline{W}$
$\overline{DAV}$
Bus slave
$\overline{DAV}$ = 0 indicates
data valid


A
B
C
D
Data
Data valid
DAV
Master
Data
Slave
DAV


A
B
C
D
E
F
Data
Data valid
DAV
ACK
Master
Data
Slave
DAV
ACK


S0
S1
S2
S3
S4
S5
S0
CLK
Address
Address valid
DS
R/W
DSACK
Data
Data valid
A
B
C
D
CPU
Memory
Address
DS
R/W
DSACK
Data