(combinatorial) or registered (sequential) function with built-in logic structures called logic cells (LC) or logic blocks (LB). Like EPROM devices, LCs can implement logic or Boolean functions using a memory to store the logic function. LCs inputs are used to address a memory containing the truth table of the function. This memory is called "*Look-Up Table*" (LUT).

Like a semi-custom gate array, a FPGA consists of a two-dimensional array of logic and memory blocks that can be connected by general interconnection resources. The interconnect comprises segments of wire, where the segment may be of various lengths.

Present in the interconnect are programmable switches that serve to connect the logic blocks to the wire segments, or one wire segment to another. These routing wires also connect to I/O's blocks. FPGA architectures differ from vendor to vendor, but in general it could be described using the following figure:

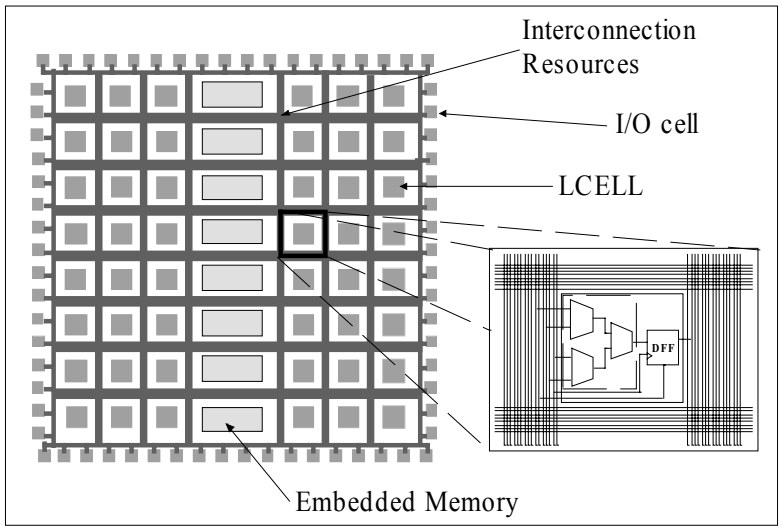

FIGURE 1.2.6. FPGA INTERNAL ARCHITECTURE

1.2.4 FPGA and Application-Specific Integrated Circuit (ASIC)

Before a description of FPGAs, It is important to understand the differences between ASICs and FPGAs.

An ASIC is a custom monolithic IC that is customized on all mask layers. There are two types of custom IC:

3. The Standard cell IC. This device is customized on all mask levels using a cell