Flex vs Stratix HW Summary – Key New Features in Stratix

- Random Logic: synchronous load/clear to each LE, dedicated cascade routing for LUTs, XOR gate for add/subtract capabilitiy
- Fast Add/Subtraction: XOR gate for add/subtract capability in one LE, carry select logic for architectural speedup of addition/subtraction
- High Level Arithmetic Functions: dedicated multiplier blocks in Stratix (18x18, signed or unsigned)
- DSP Support: configurable datapaths with dedicated multipliers and adder/accumulator (up to 56 bits)
- Memory: true dual port RAM blocks
- IO : support for new differential IO standards
- Clocking: hierarchical clock network instead of flat global clock network
- Vdd supply: Flex (versions at 5.0v, 3.3, and 2.5v). Stratix: 1.5 v.

Common Misconceptions on Homework

- "Random logic" means implementation of random number generators
  - No – "random logic" refers to the mapping of arbitrary combinational or sequential logic functions
- Flex has dedicated support for multiplication operations via EABs (embedded array blocks)
  - No, this is simply marketing spiel. An EAB is just a memory. You can implement any combinational logic function in memory, but it is usually inefficient to do so for combinational functions with many inputs. The EAB in the Flex can be configured as a 256 x 8 Memory device – 256 locations = 8 address lines, so can implement a 4x4 multiplication in the EAB. This is VERY INEFFICIENT, and making a larger multiplier by combining these together is even worse.
  - This is why Stratix added dedicated multiplier blocks.
  - Message: know how to read through marketing hype.

Common Misconceptions on Homework (cont)

- The Flex device has dual port memory
  - Again, marketing hype. The memory blocks (EABs) have only a single port on them (address + data). You can implement a dual port memory function by sharing the port between multiple devices on different clock cycles, but this is not really a dual port memory.
  - Some Stratix memory blocks implement true dual port (independent, simultaneous operations on both ports), and all implement simple dual port (a read on one port and a simultaneous write on the other port).
- The Flex and Stratix support floating point operations
  - Any programmable logic device can implement a floating point hardware unit since it is simply a combinational system. The question is EFFICIENCY. The Flex and Stratix have no inherent support for floating point hardware implementation. The 36x36 multiplier configuration supported by Stratix makes implementation of a floating point unit more efficient, but it only supplies a piece of the puzzle. It still takes a lot of other logic resources to make a complete floating point unit.

Common Misconceptions on Homework (cont)

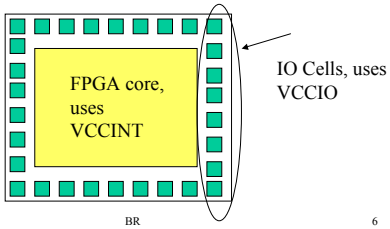
- The lowest power supply voltage for *normal operation* on the Flex and Stratix devices are negative values (I.e, -0.5 v, -2.0v).
  - First, CMOS logic does CANNOT *operate* on a negative voltage with respect to ground.
  - There are two tables in data sheets concerning voltage supply – one called 'absolute maximum ratings' and one called 'recommended operating conditions'.
  - 'Absolute maximum ratings' means what can be applied to the supply pins without damaging the device. It does not mean the device *operates* at these voltages.
  - 'Recommended operating conditions' provides the supply voltages that will give reliable, longterm device operation. There is a usually a nominal value given (I.e, 1.5 V for Stratix) with a min/max range about this point (1.425 to 1.575 v).

Common Misconceptions on Homework (cont)

- The power supply for Stratix was lowered to 1.5V to make it a low power device
  - Wrong. Stratix devices will be manufactured on a 0.13µ process. As you shrink the transistors, the maximum operating voltage for reliable, long term operation goes DOWN because the gate oxide (insulator between gate terminal and channel in a PMOS/NMOS transistor) becomes thinner and thinner. You have no choice but to lower the supply voltage – high voltages will damage this insulator (cause gate to to channel punch-thru).
  - Large Stratix FPGAs will actually be very power hungry. The large number of transistors on them and aggressive technology (0.13µ) will cause significant static power dissipation via leakage current. Everything about Stratix devices is designed for high performance clocking, which is incompatible with low power.

Common Misconceptions on Homework (cont)

- The Stratix device can operate on 3.3, 2.5, 1.8 and 1.5 v
  - These are the supported IO voltages (VCCIO), not the supply voltage (VCCINT). The IO voltage is the voltage supplied to the IO cells around the peripheral of the chip, but is not used for the chip core logic. VCCINT is used for the chip core logic.



Final Exam

- Stratix vs Flex differences
  - Look at the Stratix vs Flex lecture – short answer questions will draw heavily from this lecture
- Serial IO – will ask questions relating to this lab assignment
- Tests #1, #2 - will ask questions on this test content.
- No calculators allowed.
- Will not ask questions on Structural VHDL , Video, or Design for Test
- Extra points earned on Labs apply to test grades, but not final exam grade.
- Final grade calculation is as stated on policy, except there are only two exams.