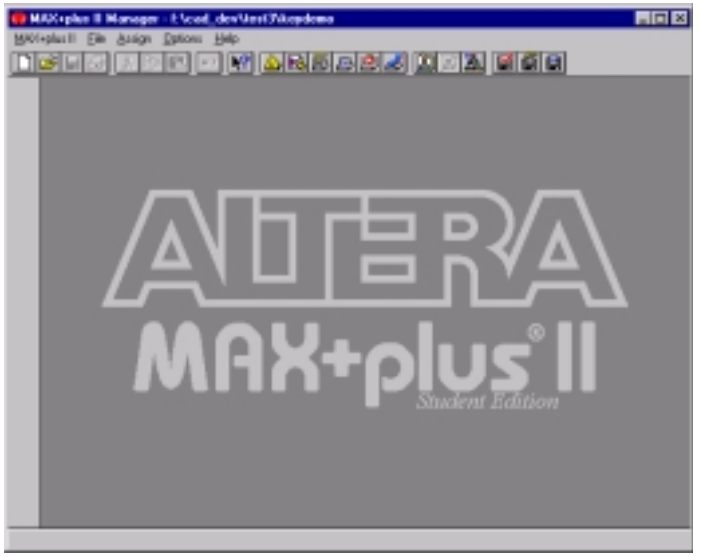
Altera Maxplus Tutorial

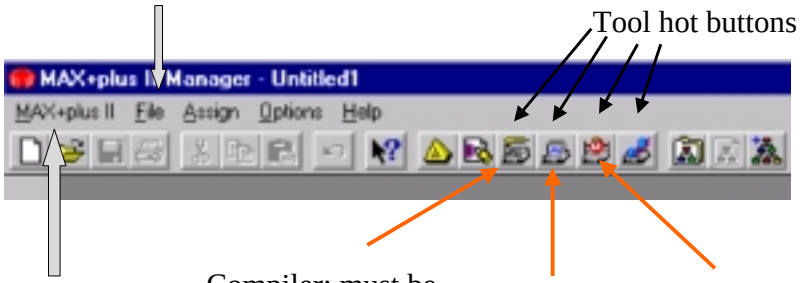
- **This is a short tutorial on Altera Max+plus II schematic capture and simulation**
- **You have the choice of using either University PCs (Zakhem, 4th floor) or your PC.**
  - I would suggest your own PC; no competition for seats, convenient, very fast if you have a 200 Mhz or better CPU and 32 Mb of memory.
  - The class WWW page will have a link that discusses home PC installation.

MAX Plus Main Window



Main Menu Bar

Create new files, open old files, set project



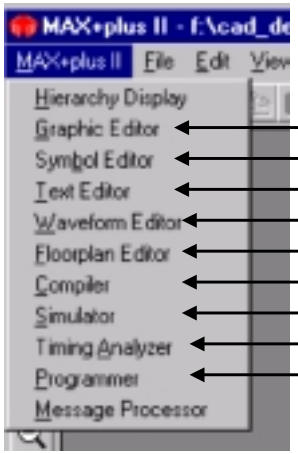
Main menu for accessing tools outside of quick buttons

Compiler: must be run on schematic or VHDL file before simulation

Simulator, waveform must have been created first.

Timing analyzer

MAX+plusII Menu



Create new schematic

Rarely used, will use Auto symbol create

Edit VHDL files

Edit/Create waveforms for simulation

View logic mapping onto FPGA

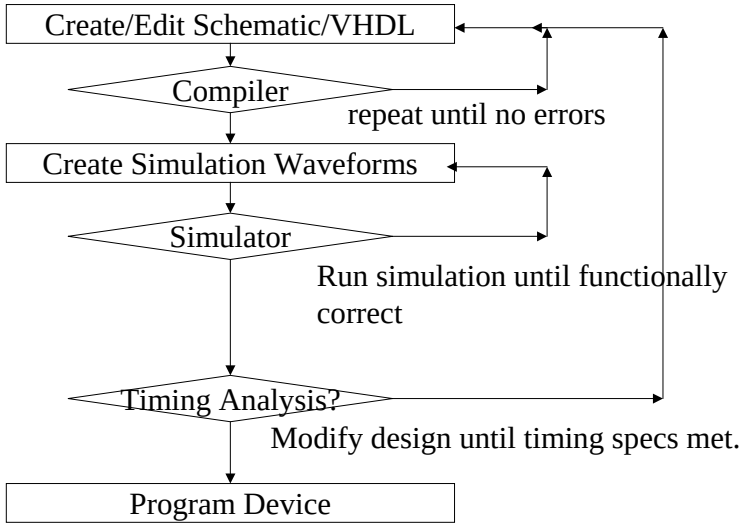
Compile/Map schematic/VHDL to FPGA

Simulate Design

Analyze Timing of Mapped design

Dowload design to FPGA

Methodology



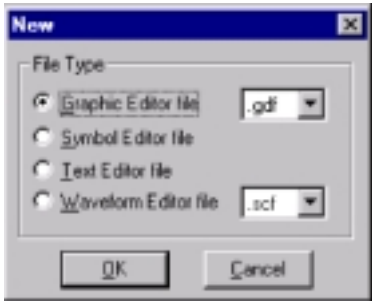
File Types

- **.gdf Schematic Files (user created, schematic editor)**
- **.vhd VHDL Files (user created, text editor)**
- **.scf Waveform files (user created, waveform editor)**
- **.rpt Report of compilation process (tool created)**
- **.acf Project configuration file, automatically generated but can be edited by user (e.g., for pin assignments)**
- **.sym Symbol files, automatically generated, can edited by user (to create a custom symbol).**

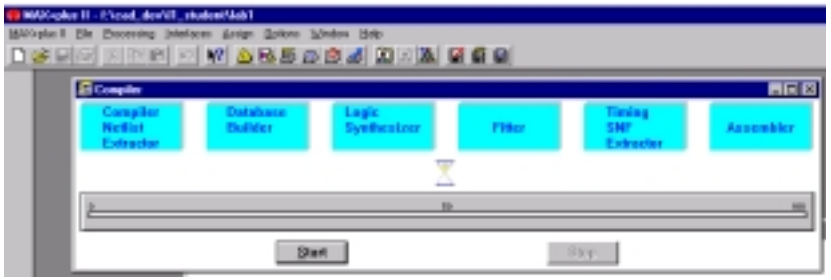
There are MANY, MANY other files automatically generated by various tools. Only the above types need to be preserved in order to keep your design; the other files can be deleted.

File Creation

To create any new file, use File -> New command from main menu, will pop up file creation menu, choose a type.



Compiler



After creating schematic or VHDL file, clicking on start button will start compilation process. After compilation is complete, can simulate design (if you have created a test waveform for the design).

Sample Schematic

A sample schematic is show below for reference.