Verilog

- Verilog is an alternative language to VHDL for specifying RTL for logic synthesis
- VHDL similar to Ada programming language in syntax
- · Verilog similar to C/Pascal programming language
- VHDL more popular with European companies, Verilog more popular with US companies.
- VHDL more 'verbose' than Verilog.
- Verilog and VHDL do RTL modeling equally well.

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Verilog Vs. VHDL

- Verilog and VHDL are equivalent for RTL modeling (code that will be synthesized).
- For high level behavioral modeling, VHDL is better
 Verilog does not have ability to define new data types
 - Other missing features for high level modeling
- Verilog has built-in gate level and transistor level primitives
 - Verilog much better than VHDL at below the RTL level.
- Bottom Line: You should know both!!!!!

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11