P4C148, P4C149
ULTRA HIGH SPEED 1K x 4
STATIC CMOS RAMS

FEATURES

- **Full CMOS, 6T Cell**
- **High Speed (Equal Access and Cycle Times)**
  - **10/12/15/20/25 ns (Commercial)**
  - **15/20/25/35 ns (P4C148 Military)**
- **Low Power Operation**
  - **715 mW Active –10 (Commecial)**
  - **550 mW Active –25 (Commercial)**
  - **110 mW Standby (TTL Input) P4C148**
  - **55 mW Standby (CMOS Input) P4C148**
- **Single 5V ± 10% Power Supply**
- **Two Options**
  - **P4C148 Low Power Standby Mode**
  - **P4C149 Fast Chip Select Control**
- **Common Input/Output Ports**
- **Three-State Outputs**
- **Fully TTL Compatible Inputs and Outputs**
- **Standard Pinout (JEDEC Approved)**
  - **18 Pin 300 mil DIP**

DESCRIPTION

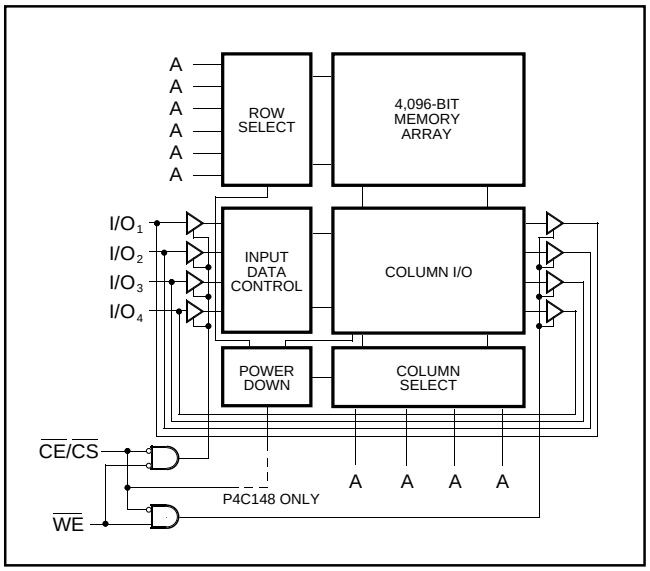
The P4C148 and P4C149 are 4,096-bit ultra high-speed static RAMs organized as 1K x 4. Both devices have common input/output ports. The P4C148 enters the standby mode when the chip enable ($\overline{CE}$) goes HIGH; with CMOS input levels, power consumption is extremely low in this mode. The P4C149 features a fast chip select capability using $\overline{CS}$. The CMOS memories require no clocks or refreshing, and have equal access and cycle times. Inputs are fully TTL-compatible. The RAMs operate from a single 5V ± 10% tolerance power supply.

Access times as fast as 10 nanoseconds are available, permitting greatly enhanced system operating speeds.

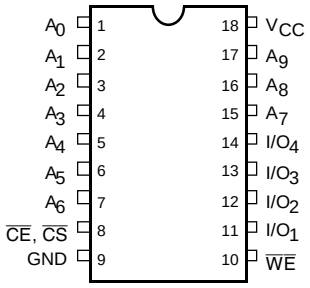
CMOS is used to reduce power consumption when active; for the P4C148, consumption is further reduced in the standby mode.

The P4C148 and P4C149 are available in 18-pin 300 mil DIP packages providing excellent board level densities.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



P4C148 DIP (P1, D1)
P4C149 DIP (P1)
TOP VIEW