CdL Scienza dei Materiali - Fisica delle Nanotecnologie - a.a. 2004/05

Appunti & trasparenze - Parte 1

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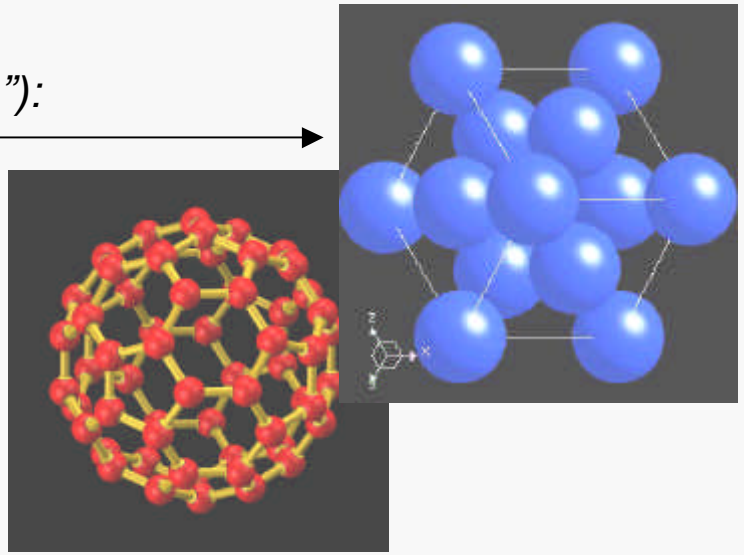
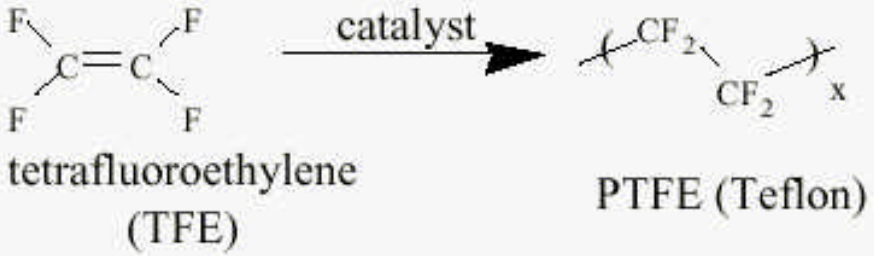
Generalità sulle nanotecnologie, ambito scientifico e tecnologico, motivazioni, prospettive,cenni su dispositivi convenzionali micro- e nanoelettronici

4/10/2004 - 9.30 + 2 - ITI L

Il “nanomondo”: dimensioni tipiche submicrometriche

Dimensioni sub-nanometriche in *natura (“limite inf.”):*
- passo reticolare cristalli ~ alcuni Å (Si: 5.431 Å)
- “diametro” molecola fullerene ~ 7 Å
- “dimensioni lineari” di un monomero (polimero)





tetrafluoroethylene (TFE)

PTFE (Teflon)

Obiettivi “tecnologici”: *realizzare, studiare e sfruttare* nanostrutture:
- crescita (asse z);
- definizione laterale (asse x e/o y)

See the Feynman’s speech (29/12/1959!!) at http://www.zyvex.com/nanotech/feynman.html

NANOTECNOLOGIA

“Utilità” delle nanostrutture

Impiego di nanostrutture prodotte artificialmente (e intenzionalmente) dalla tecnologia ha utilità in moltissimi settorI. Qualche esempio:

-Materiali strutturali (nanocompositi con proprietà meccaniche superiori,…)

-Materiali tribologici e adesivi (lubrificanti al fullerene o diamantati,…)

-Applicazioni biomediche (marcatori a quantum dots, drugs dispensers, etc.)

-….

Esempio “storico” (IV sec AC) di interesse “artistico” per l’impiego di nanoparticelle d’oro in matrice vetrosa

Lycurgus Cup in Roman times

Dr. Juen-Kai Wang

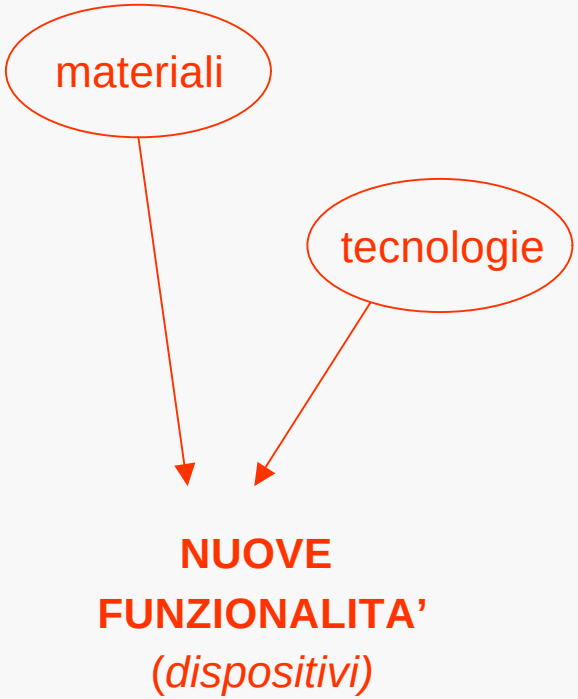
The glass appears green in daylight (reflected light), but red when the light is transmitted from the inside of the vessel.

The Lycurgus Cup, Roman (4th century AD), British Museum (www.thebritishmuseum.ac.uk)
*F. E. Wagner et al., Nature **407**, 691 (2000).*

Motivazioni ed ambito

Da C.P.Poole and F.J.Owens, Introd. to nanotechnology (Wiley, 2003)

The current widespread interest in nanotechnology dates back to the years 1996 to 1998 when a panel under the auspices of the World Technology Evaluation Center (WTEC), funded by the National Science Foundation and other federal agencies, undertook a world-wide study of research and development in the area of nano-technology, with the purpose of assessing its potential for technological innovation. Nanotechnology is based on the recognition that particles less than the size of 100 nanometers (a nanometer is a billionth of a meter) impart to nanostructures built from them new properties and behavior. This happens because particles which are smaller than the characteristic lengths associated with particular phenomena often display new chemistry and physics, leading to new behavior which depends on the size. So, for example, the electronic structure, conductivity, reactivity, melting temperature, and mechanical properties have all been observed to change when particles become smaller than a critical size. The dependence of the behavior on the particle sizes can allow one to engineer their properties. The WTEC study concluded that this technology has enormous potential to contribute to significant advances over a wide and diverse range of technological areas ranging from producing stronger and lighter materials, to shortening the delivery time of nano structured pharmaceuticals to the body's circulatory system, increasing the storage capacity of magnetic tapes, and providing faster switches for computers. Recommendations made by this and subsequent panels have led to the appropriation of very high levels of funding in recent years. The research area of nanotechnology is interdisciplinary,



Settore tradizionalmente trainante: (micro)elettronica

Miniaturizzazione ⇒ dimensioni compatte, aumento potenza (capacità trattamento ed immagazzinamento dati), diminuzione consumi, *motivi commerciali*...

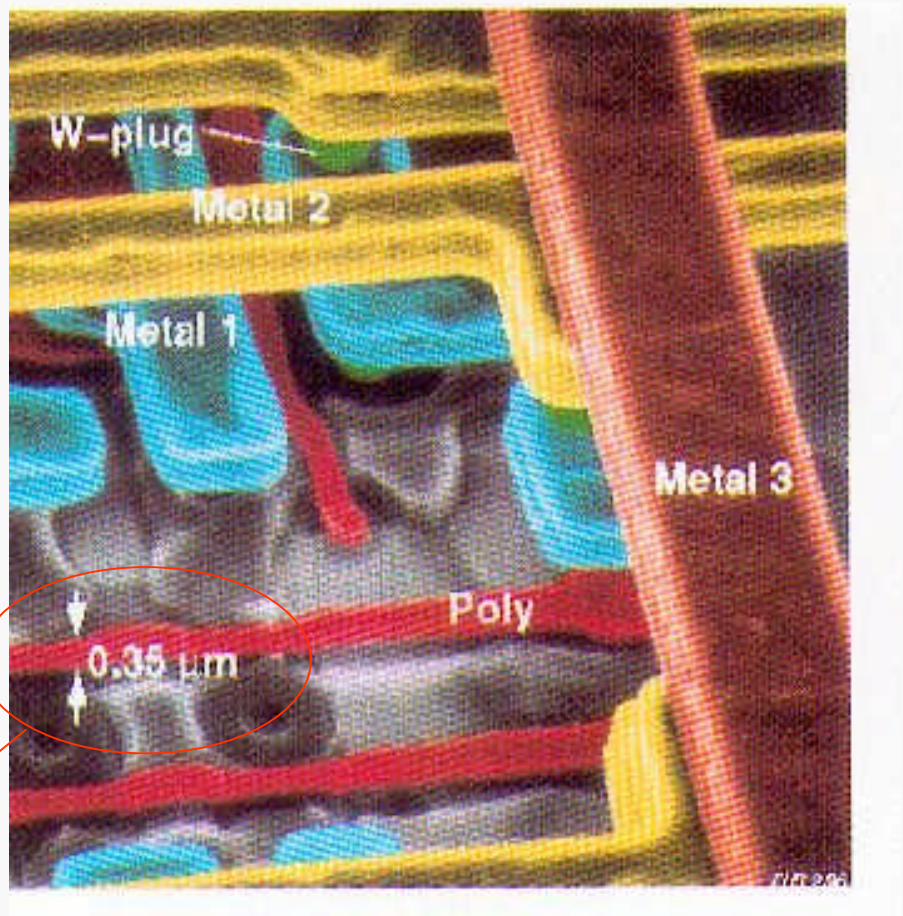
Realizzazione pratica di device a più livelli (con interconnessioni)

Miniaturizzazione dispositivo

⇩

Aumento potenza (di calcolo in CPU, di storage in memorie), meno consumo, più velocità,…

Miniaturizzazione vs prestazioni
Esempio: velocità (basso RC):
⇒ capacità (C ~ S/h)
⇒ resistenza (R ~ L/S)



Feature size (tipicamente è fwhm delle strutture più piccole)

Miniaturizzazione Û prestazioni

“Legge” di Moore:
la “miniaturizzazione”
aumenta
di un fattore 4 ogni 3 anni

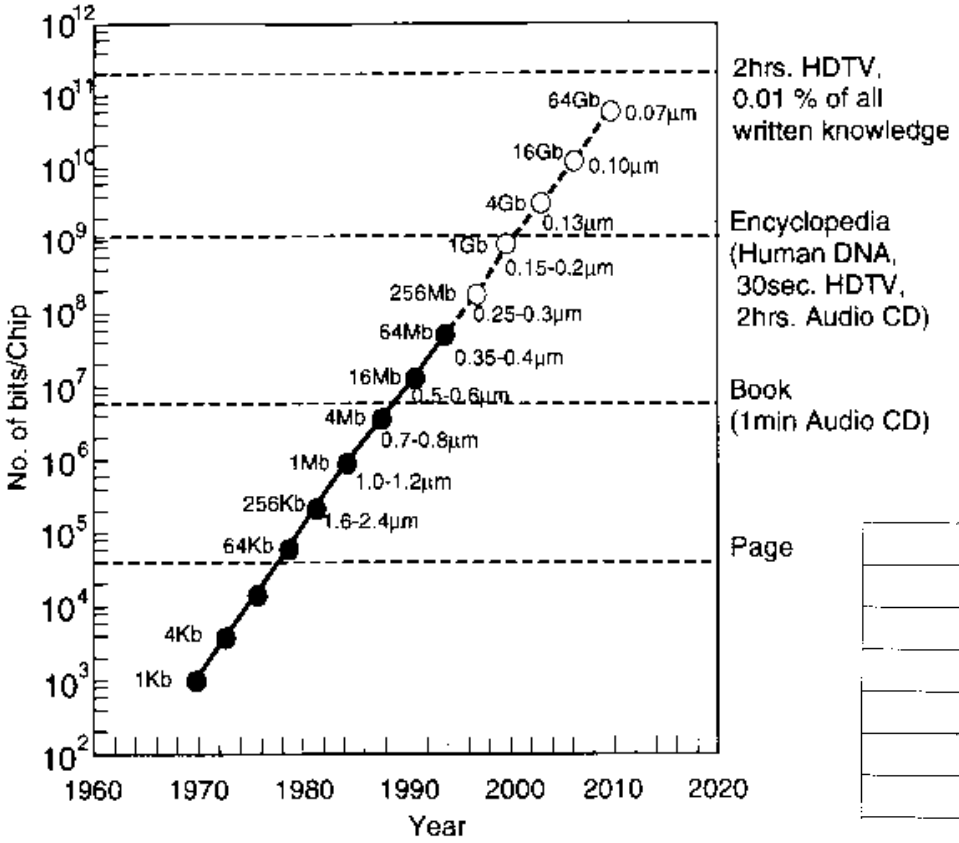


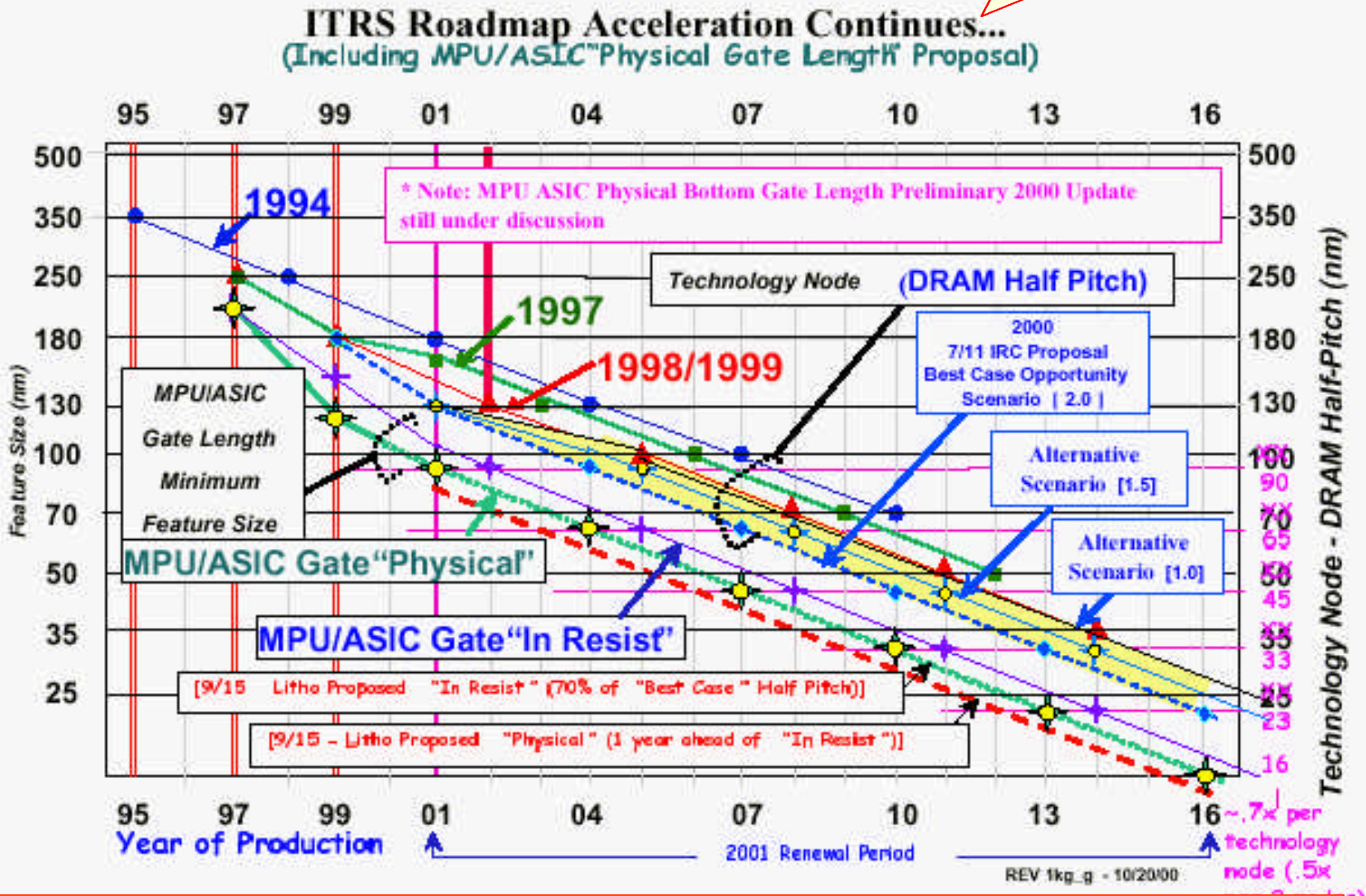
FIGURE 2. The complexity curve adapted from Moore[7] showing the time of the information storage capacity of silicon DRAM chips. The tabulated based on publications in the ISSCC Technical Digests. Tl (indicated by the dotted line) are based on the SIA Roadmap. The appl tion storage capacity of an encyclopedia, human DNA, two hours 30 seconds of HDTV, a book, 1 minute of Audio CD, and a page are indicated for reference.

TASK:	MIPS
Speech Recognition (numbers)	≈50
Digital Signal Processor (audio)	≈50
Cellular Phone	≈50
Personal Computer	≈100
Video Games	≈200
HDTV	≈1000
Color FAX	≈7000
Speech Recognition (5000 words)	≈10,000
MPEG2 Encoder	≈20,000
multimedia DSP	≈50,000
Video Graphics (Ray Trace)	$\approx 10^9$
Secondary Structure of genome	$\approx 10^{12}$

Limiti delle tecnologie attuali?
Dispositivi con *nuove funzionalità?*
Nuovi materiali?

Roadmaps per il futuro…

See http://public.itrs.net

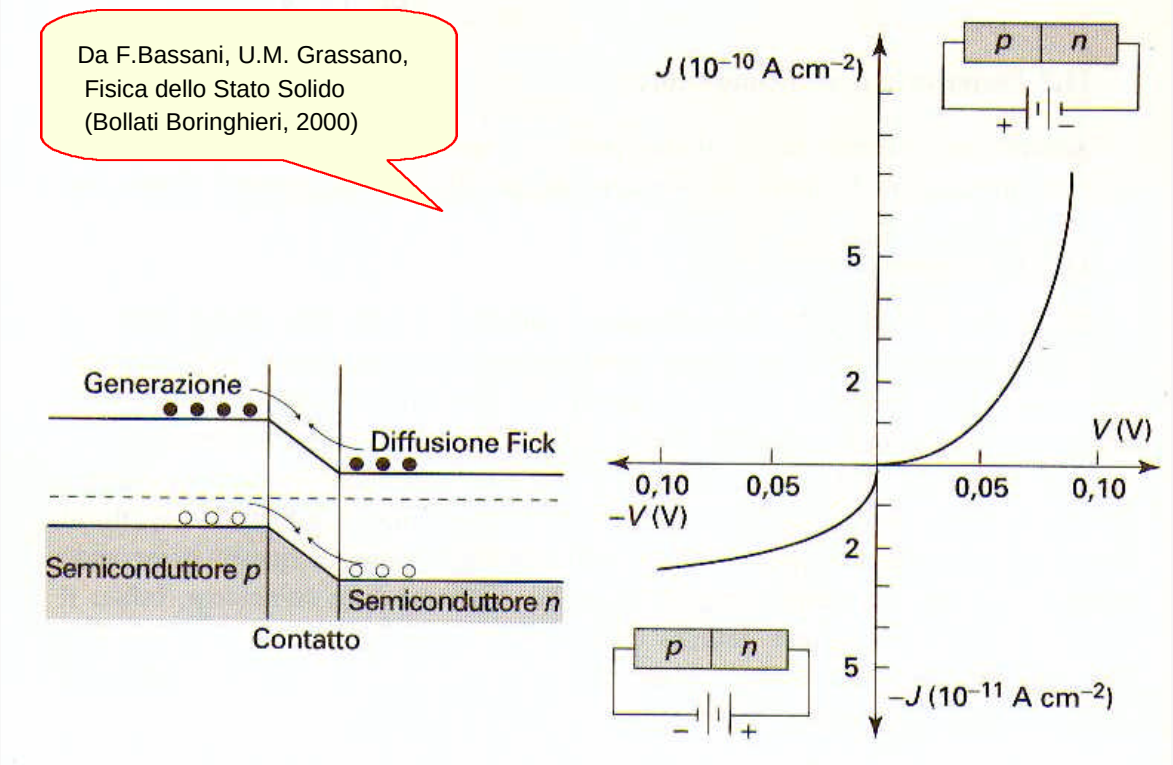


Alla fine, la natura atomica della materia porrà un limite (~nanometro?)

*ASIC: application-specific integrated circuit

Le basi dei dispositivi elettronici: qualche richiamo

Tecnologia tradizionale (anni '50): semiconduttori (inorganici) con diverso drogaggio



In condizioni di equilibrio (senza campo applicato), le cariche si ridistribuiscono in modo da creare una regione attorno alla **giunzione** che è "vuota di cariche"

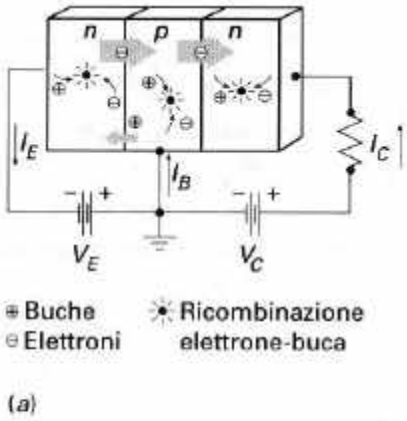
$\Rightarrow$ si crea una **barriera di potenziale** per le cariche

$\Rightarrow$ si ha trasporto solo **polarizzando direttamente** la giunzione

$\Rightarrow$ comportamento **rettificante** della giunzione pn, o np

Nota: si ha comportamento rettificante anche nella giunzione semiconduttore/metallo (giunzione Schottky)!

Richiami sul funzionamento di un transistor bipolare



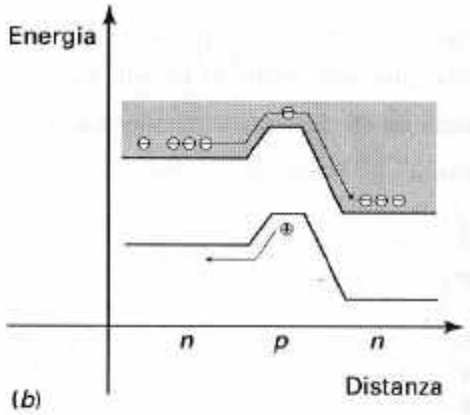


Figura 11.16
Transistor $n-p-n$, con i relativi simboli per indicare la corrente di emettitore (I_E), di collettore (I_C), e la corrente di base (I_B). (*a*) Indicazione degli stati di polarizzazione e dei flussi di corrente (buche ed elettroni). (*b*) Posizionamento delle bande in presenza di un campo (diretto per la giunzione $n-p$).

In un transistor $n-p-n$ si ha ad un estremo l'emettitore di elettroni, i quali entrano dal contatto nel semiconduttore n e all'altro estremo del secondo semiconduttore n vi è il collettore, mentre il semiconduttore p intermedio, molto più sottile degli altri, è chiamato base. All'equilibrio senza polarizzazione non si ha passaggio di corrente perché $I_g^0 = I_r^0$ a entrambe le giunzioni. Basta però applicare una differenza di potenziale tra il collettore e l'emettitore e controllare il potenziale della base per ottenere un'amplificazione di tensione. Illustriamo il funzionamento di tale transistor riferendoci alla fig. 11.16. In questo schema si hanno due circuiti. Uno è il circuito $e-b$ (emettitore-base) che è rettificante per le ragioni esposte precedentemente a proposito del diodo. L'altro è un circuito $b-c$ (base-collettore) che da solo lascerebbe passare poca corrente perché il potenziale è tale da aumentare la barriera di potenziale. In presenza del circuito precedente però molti più elettroni arrivano al semiconduttore p per l'effetto dell'abbassamento

Da F.Bassani, U.M. Grassano,
Fisica dello Stato Solido
(Bollati Boringhieri, 2000)

della barriera al confine $n-p$ e tali elettroni non trovano ostacoli a proseguire attraverso la zona n ed arrivare al collettore. Questo produce perciò amplificazione di potenza nel circuito $b-c$ rispetto al circuito $e-b$.

La corrente che passa per $n-p$ è I_e:

$$I_e = I_g^0\left(e^{\frac{eV_e}{kT}} - 1\right), \tag{11.64}$$

dove V_e è il potenziale dell'emettitore. La corrente che passa al collettore I_c sarà

$$I_c = I_e - I_b, \tag{11.65}$$

dove I_b, corrente di base, è piccola in ogni caso. Se la base è a terra si può ritenere $I_b \simeq 0$ e la corrente raccolta al collettore sarà data dalla (11.64). Non c'è in questo caso amplificazione di corrente tra emettitore e collettore, ma c'è grande amplificazione di tensione (o di potenza), perché la stessa corrente passa da un circuito d'ingresso a bassa impedenza (giunzione con polarizzazione diretta) ad un circuito d'uscita a grande impedenza (giunzione con polarizzazione inversa) e qui scorre attraverso una grande resistenza R_L. Dunque un transistor a base comune si comporta come un amplificatore di tensione (o di potenza).

Se il transistor è collegato con emettitore comune (a terra), si comporta come un amplificatore di corrente (vedi fig. 11.17). Come si è visto prima, quasi tutta la corrente I_e della giunzione emettitore-base (polarizzata direttamente) raggiunge il collettore, così si può scrivere

$$I_c = \alpha I_e \tag{11.66a}$$

Tecnologie/materiali/dispositivi

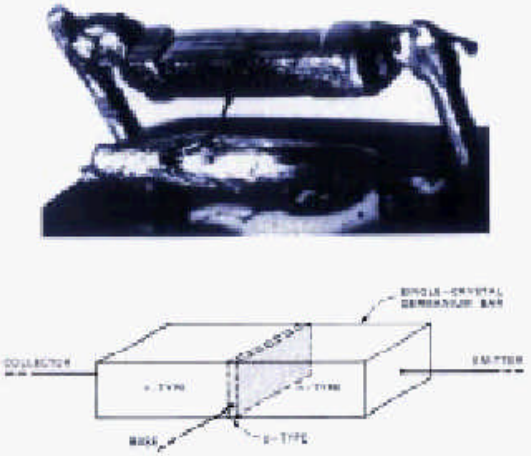


Figure 1 – The first transistors: (a) the point contact transistor of Brattain and Bardeen, 1947 (left); (b) the junction transistor of Shockley, Morgan, Sparks, and Teal, 1950 (right).

La tecnologia degli anni ‘50 si basava su elementi macroscopici (barrette di materiale semiconduttore drogato) e non si prestava a miniaturizzazione.

Negli anni ‘70, grazie a innovazioni tecniche, si diffonde la tecnologia planare, fondata sulla *crescita (epitassiale) di film sottili*

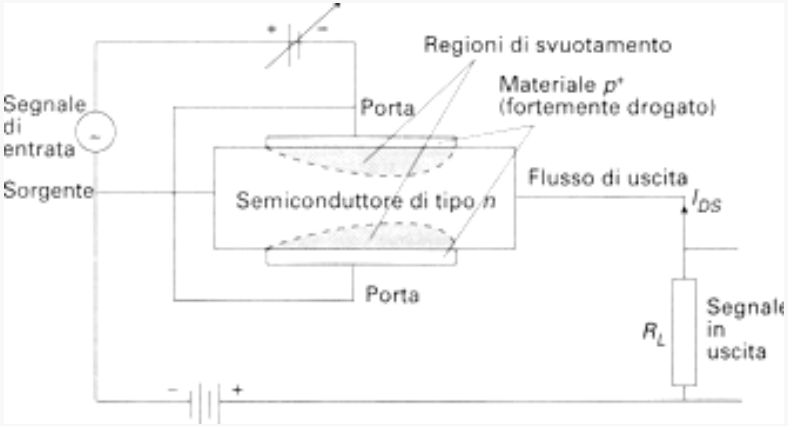
⇩

MOS-FET

Cenni sul MOS-FET ("convenzionale")

Elemento di base dei dispositivi Microelettronici attuali: FET (MOS-FET)

(elemento *attivo*: la tensione al gate controlla la corrente drain-source)



Ingrediente fondamentale per:
- CPU/MPU (funzioni logiche)
- memorie (storage)

	MEMORY	LOGIC
	High volume DRAM/Flash	*High volume: Microprocessor*
transistors/cm^2	64 M	4 M
On-Chip Frequency (MHz)	150	150–300
Chip size (mm^2)	190	250
Number of Defects	560	425
Number of Package Pins/Balls	30–60	512
Interconnect Density (Metal 1) (m/cm^2/level)	60	35
Number of Metal Interconnect Levels	2	4–5
Interconnect Length (m)	–	380
Maximum power dissipation (W/die)	3–5	5–80

Idea di base: il trasporto di cariche da **source** a **drain** è controllato dal campo elettrico generato applicando una ddp tra **gate** e substrato

Elemento "attivo" (tre terminali!) in cui V_{Gate} controlla $I_{ource\text{-}drain}$
(diverso e più efficace di transistor biplare in cui $I_{base\text{-}collettrore}$ controlla $I_{collettore\text{-}emettitore}$)

MOS-FET: costruzione planare (film sottili) ⇒ *miniaturizzazione lungo z*

Realizzazione del MOS-FET

MOS-FET significa: Metal Oxide Semiconductor Field Effect Transistor

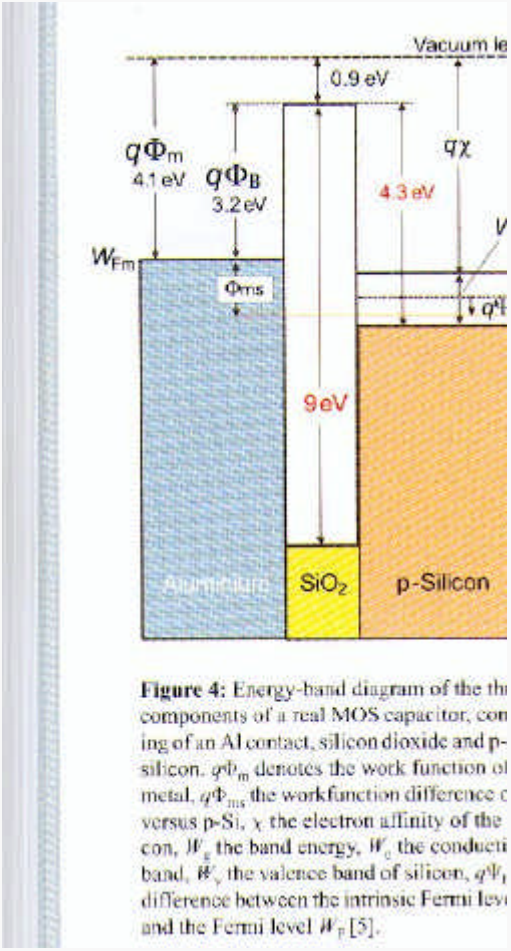


Figure 4: Energy-band diagram of the th components of a real MOS capacitor, con ing of an Al contact, silicon dioxide and p- silicon. $q\Phi_m$ denotes the work function o metal, $q\Phi_{ms}$ the workfunction difference versus p-Si, χ the electron affinity of the con, W_g the band energy, W_c the conducti band, W_v the valence band of silicon, $q\Psi_i$ difference between the intrinsic Fermi lev and the Fermi level W_F [5].

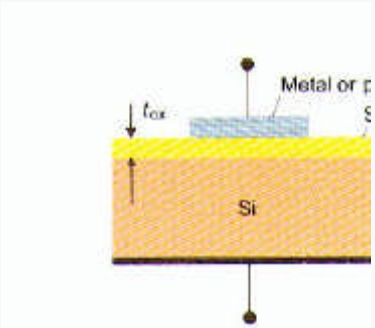


Figure 3: Schematic structur of a MOS capacitor.

Da R. Waser Ed., Nanoelectronics and information technology (Wiley-VCH, 2003)

Elemento di base è condensatore MOS
Strato di ossido deve essere sottile per garantire campi elevati con basse ddp (E=V/d!!)
(impiego di materiali “ad alto k”, cioè con alta costante dielettrica)

Dettagli di operazione di un condensatore MOS

2.1 MOS Capacitor

Figure 3 shows the structure of a MOS capacitor with the three components, the metal or polysilicon contact, the silicon dioxide with a thickness t_{ox} and the silicon. The corresponding band diagram is shown in Figure 4. Due to the 9 eV bandgap of the silicon dioxide and the large band offsets relative to the silicon, the potential barrier between the conduction band of the silicon and the silicon dioxide is large (≈ 3.1 eV). This barrier crucially controls possible charge transport through the dielectric layer in the presence of an applied voltage, and thus, determines the reliability of the dielectric-semiconductor interface. Frequently poly-Si is used as a contact material instead of a metal. For p-type poly-Si the work function is $\Phi_s = \chi + W_g/2q + \Psi_B \approx 4$ eV, where χ denotes the electron affinity, W_g the band gap energy, Ψ_B the difference between the Fermi potential W_F and the intrinsic potential W_i.

The energy band diagram of an ideal MOS capacitor with a p-type semiconductor is shown in Figure 5 ($q\Phi_{ms}$ is assumed to be zero, see Figure 4). When a negative gate potential $V_G < 0$ is applied the Fermi level of the metal increases and an electric field is created in the SiO_2, indicated by the slope of the conduction band of the SiO_2, and in the silicon. Because of the low carrier concentration the Si bands bend upwards at the SiO_2 interface, leading to an **accumulation** of excess holes. In order to conserve charge, an equivalent number of electrons is accumulated at the metal side of the MOS capacitor.

When a positive potential is applied at the gate contact, its Fermi level moves down leading to band bending in the silicon in the downward direction. As a consequence, the hole concentration near the interface decreases. This status is called the **depletion condition**. Charge neutrality requires the induction of an equivalent amount of positive charge at the metal-oxide interface Q_M as negative charge in the semiconductor Q_S, explicitly,

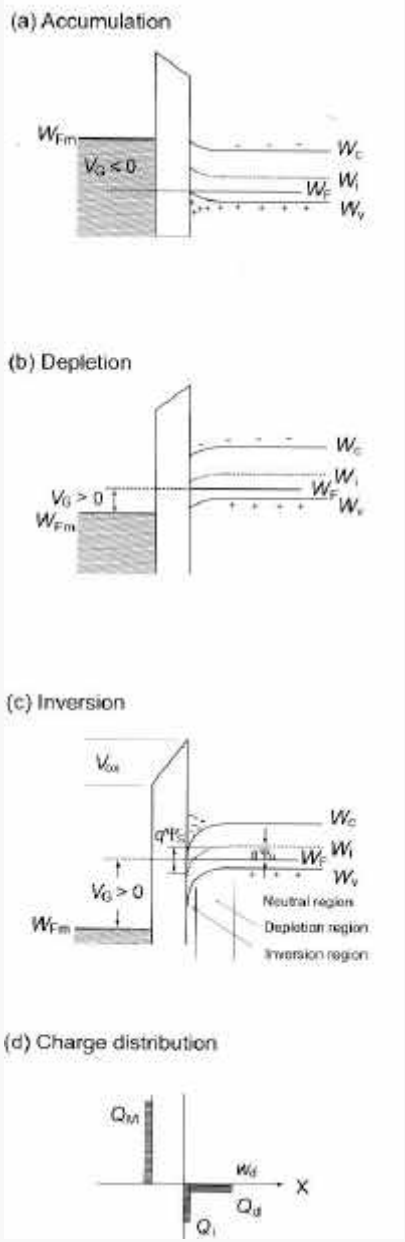
$$Q = -Q_M \text{ with } Q_S = Q_d \qquad (1$$

where Q_d originates from the ionized donor states. A further increase of the positive gate potential, enhances band bending such that at a certain gate potential the intrinsic Fermi level crosses the Fermi level as shown in Figure 5c. Energetically, it becomes now favourable for electrons to populate the newly created surface channel. The surface behaves like an n-type semiconductor where the doping was created by inverting the original p-type silicon with an applied field. This condition is called **weak inversion** and the corresponding onset gate voltage the threshold voltage V_t. The negative charge at the semiconductor interface Q_S consists of inversion charge Q_i (electrons) and ionized acceptors Q_d (Figure 5d)

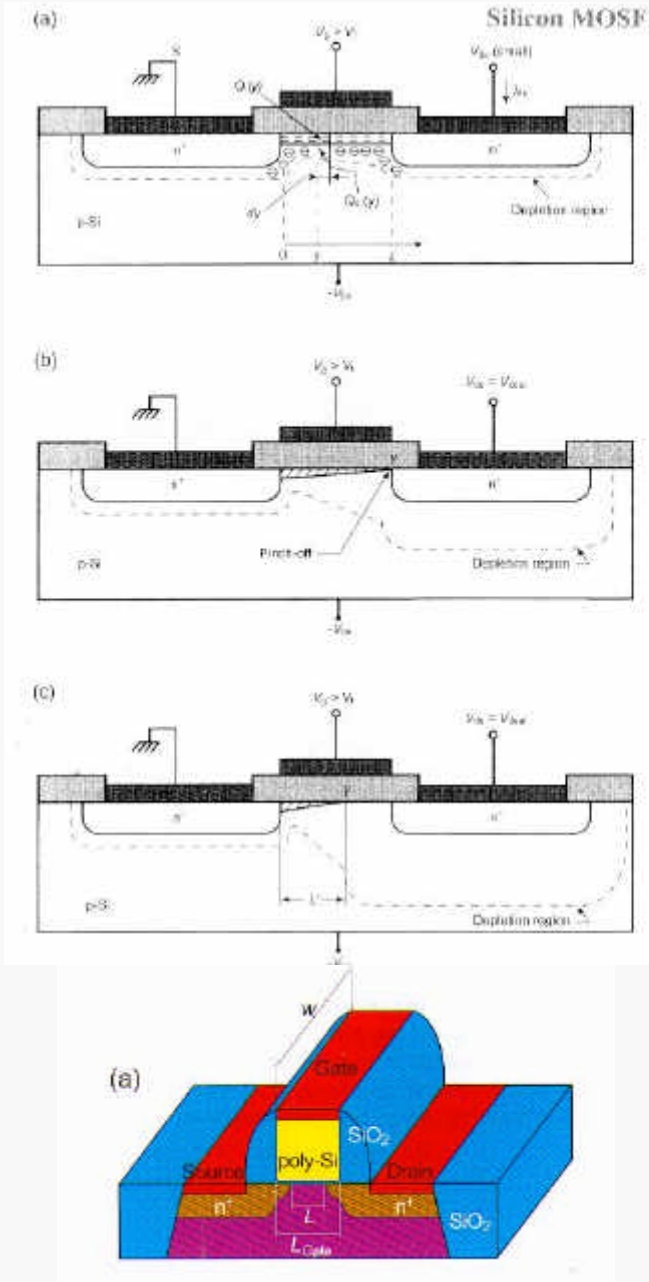
$$Q = Q_i + Q_d \qquad (2$$

As indicated in Figure 5c, three regions develop within the semiconductor: a shallow inversion region, a depletion region with a maximum depth w_d and deeper in the substrate a neutral region. A further increase of the potential yields to **strong inversion** when the concentration of the electrons exceeds the hole concentration in the substrate ($Q_i > Q_d$). Then, the gate voltage V_G can be expressed by

$$V_G = V_{ox} + \psi_S = -\frac{Q_S}{C_{ox}} + \psi_S \qquad (3$$



Dettagli di operazione di un MOS-FET



Silicon MOSFETs - Novel Materials and Alternative Concepts

Figure 8: MOSFET operation at a gate voltage $V_G > V_t$ with increasing drain voltage V_{ds}.
(a) At low drain voltages the transistor is in the linear range. Q_i and Q_d are the inversion and the depletion charges, respectively.
(b) shows the pinch-off condition with the pinch-off point Y.
(c) saturation regime where the effective channel length is reduced to L' [6]

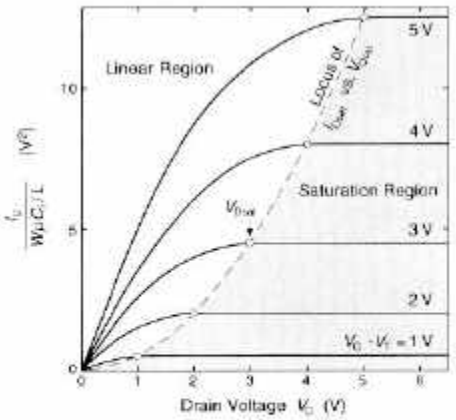


Figure 9: Idealized *I-V* curves of a MOSFET. The dashed line indicates the locus of I_{Dsat} vs. V_{dsat} [6].

For the operation of the transistor a gate and a drain voltage are applied. A sufficiently large positive gate potential V_G induces a conducting inversion layer between the source and drain contacts as discussed for the MOS capacitor. When an additional drain voltage is applied, a current flows from source to drain along the dielectric/silicon interface. Figure 8 illustrates the operation of the MOSFET at various gate and drain voltages. At low drain voltages (Figure 8a) the drain current increases linearly as shown in the *I-V* curves of Figure 9. The channel acts as a resistor. Q_i and Q_d are the inversion and the depletion charge in Figure 8a. Since the drain-substrate n^+-p-diode is under reverse bias, the depletion region increases below the n^+-drain contact and extends under the gate region with increasing drain voltage (Figure 8a - c). Thus the quasi Fermi level of the drain is qV_D lower than the quasi-Fermi level in the p-type substrate so that inversion can no longer occur near the drain although the bands at the surface are bent (see Figure 5c). As a consequence the inversion charge at the drain side approaches zero. This condition is called **pinch-off** and the corresponding drain voltage the saturation drain voltage (Figure 8b). Since the channel resistance is increased, the drain current saturates (saturation region). The pinch-off point, determined by V_{Dsat}, moves towards the source contact with increasing drain voltage. The carriers now drift down the conducting channel and are injected into the surface depletion region at the pinch-off point near the drain (Figure 8c).

MOS-FET e miniaturizzazione

How many transistors can dance on the head of a chip only 66 millimeters square? Over 58 million, thanks to IBM's sophisticated process technology that builds them just 90 nanometers wide. Such superior technology developments turbo-charge the G5 processor to speeds of up to 2.5GHz.

http://www.apple.com

To get electronics so small requires miniaturization breakthroughs, and IBM's dedication to basic scientific research makes these advances possible. For instance, the company began researching copper as an interconnect method over 25 years ago, but the technique wasn't practical until just recently.

One in 58 Million. A transistor just 90nm wide (yellow) on substrate of SOI (blue) with copper interconnects (gray). Layers of nitride (brown) and oxide (green) insulate it from its brethren. Magnified 146,000 times.

So Small

Transistors on the PowerPC G5 hold a charge to let the system make logic decisions based on whether the transistor is on or off. Using a 90nm process for even greater performance, IBM builds these devices just .00000009 meters wide on a layer of silicon on insulator. The 58 million transistors themselves are connected by over 400 meters of copper wire that's less than 1/1000th the width of a strand of your hair. Tiny paths mean less time to complete a sequence, since the

Necessità di film sottili per creare lo strato di ossido

Impiego di litografie per definire lateralmente la struttura del MOS-FET

Realizzazione pratica di un MOSFET nanodimensionato

Da G. Timp, Nanotechnology (Springer-Verlag, 1999)

Esempio di HRTEM

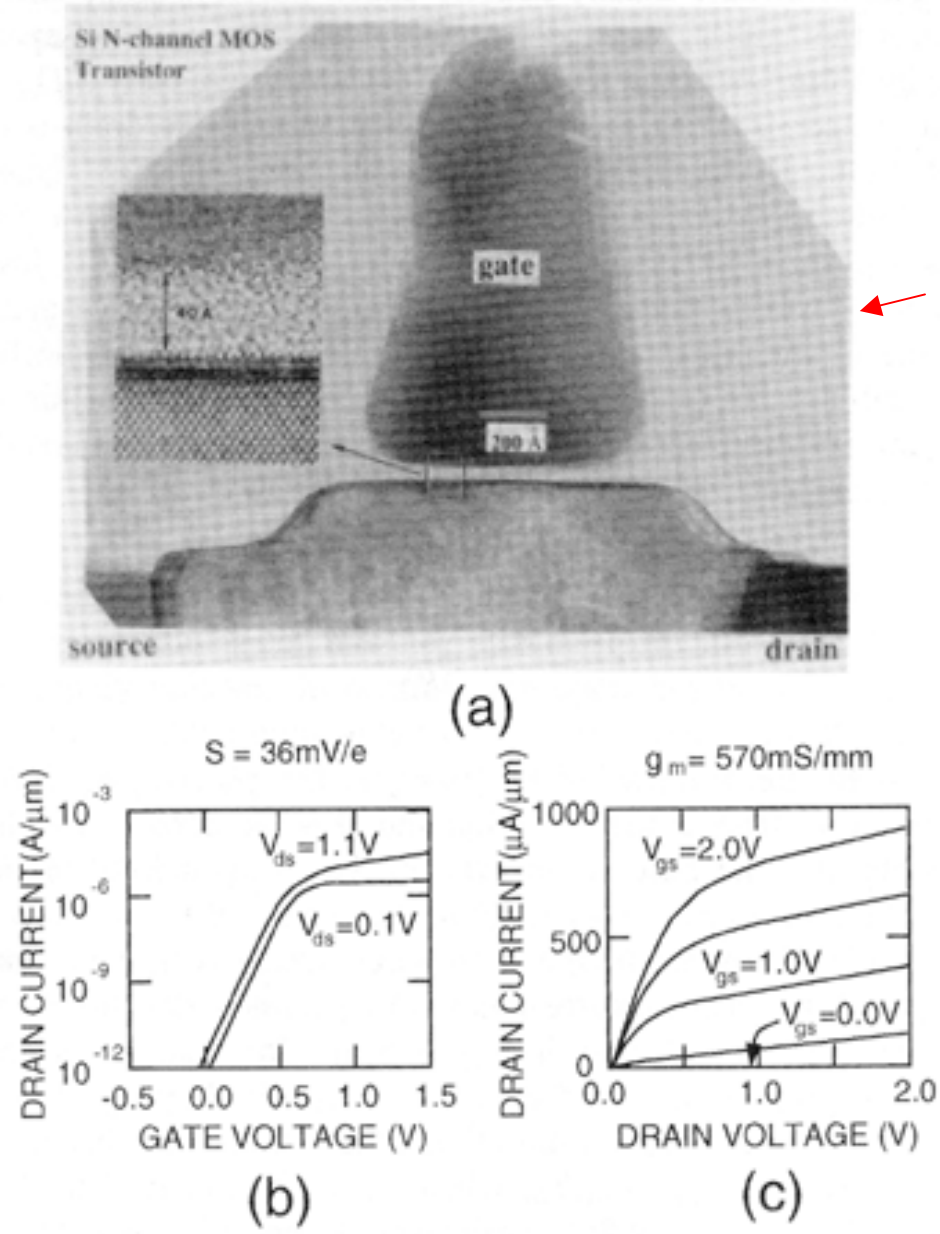


FIGURE 6. (a) A high-resolution transmission electron micrograph of a cross-section of an N-MOSFET with a gate length of 0.13 μm adapted from[27] and through the courtesy of Y. Kim. The channel is less than 400 atoms long. The inset shows a lattice image of the channel region of this device. (b) and (c) represent the measured subthreshold and drain characteristics found at room temperature for an N-MOS transistor like that shown in (a). From these measurement it can be inferred that the transconductance is approximately 570 μS/μm, and the subthreshold slope, S = 36 mV per e-fold change in I_D or 84mV/decade, and the threshold voltage is V_t =0.45 V.

Difficoltà con tecnologie e materiali tradizionali

- In order to maintain the progress of Moore's Law, the 2001 ITRS envisions **more aggressive scaling than projected in prior roadmaps**. For example, dynamic random access memory chips will feature critical dimensions of 90 nanometers in 2004, which is both smaller and sooner than the 100 nanometers projected for 2005 in the roadmap published just two years ago. Similarly, microprocessor transistor gate lengths – a critical dimension that affects the processor's speed -- will be just 25 nanometers in 2007, six years sooner than expected in the 1999 version of the roadmap. (Note: a nanometer is one-billionth of a meter. A human hair is 100,000 nanometers in width, and a red blood cell is 5,000 nanometers in width.)

- **We are beginning to reach the fundamental limits of the materials used in the planar CMOS process**, the process that has been the basis for the semiconductor industry for the past 30 years. Further improvements in the planar CMOS process can continue for the next five to ten years by introducing new materials into the basic CMOS structure. However as the ITRS looks forward 10-15 years, it becomes evident that even with the introduction of new materials, most of the known technological capabilities of the CMOS device structure will approach or have reached their limits. In order to continue to drive information technology advances, it becomes necessary to investigate new devices that may provide more cost-effective alternative to planar CMOS in this timeframe.

Previsioni per il 2005:
- Dimensioni delle celle di memoria (DRAM) sotto i 100 nm
- Lunghezza del gate in MOSFET sotto 25 nm

Limitazioni con materiali "tradizionali" (es., Silicio)

Limitazioni con tecniche "tradizionali" (es., optical lithography, maschere,...)

Da www.sia-online.org

What are examples of the difficult challenges that may impede progress in the near term (through 2007)?

There are dozens of challenges outlined in the ITRS. One example is the difficulty of making the **mask** used to transfer the integrated circuit layout designs onto future chips. As the layout designs require manufacturing transistors with finer line-widths it becomes progressively more difficult to accurately control the line-widths (e.g. a difference of a few nanometers separates success from failure.) Another difficult challenge is the prompt development of new **metrology** tools to accurately perform critical measurements as new materials, processes, and device structures are introduced. A third example is the difficulties associated with depositing metal into deep and narrow holes etched into the chip. Billions of these holes must be built on each chip to **interconnect** the billions of individual transistors on the chip.

What are examples of the long range (2008-2016) challenges?

Again, the ITRS lists dozens of technical barriers that must be overcome. For example, **optical lithography** falls short of meeting the tough requirements expected after 2010, requiring the introduction of next generation lithography tools such as extreme ultraviolet lithography and electron projection lithography. These new tools will require development of a totally new infrastructure. Breakthroughs are also needed to **interconnect** all of the transistors required on a single chip. These breakthroughs might include optical or wireless connections within a chip rather than today's electronic/metal interconnect.

Proprietà di trasporto elettronico in sistemi 2D (film sottili): effetti classici in film conduttori, semiconduttori ed isolanti

Proprietà di trasporto (elettronico): richiami

Modello elementare (Drude)

"Legge di Ohm": $\mathbf{J} = \sigma \mathbf{E}$

$\sigma = n e^2 \tau / m^*$

τ : tempo fra *collisioni*

m^* : massa efficace

Tra un "urto" e l'altro la velocità di drift è:

$v_d = \tau\, eE/m^*$

ma $\mathbf{J} = n e \mathbf{v_d}$

da cui: $\sigma = n e^2 \tau / m^*$

Classicamente:

urti con ioni (o tra elettroni) e velocità termica

Quantisticamente:

perdita simmetria traslazionale f.ne d'onda

(es. per interazione con fononi) e velocità di Fermi

Effetto Hall **classico** per misura di segno e valore della conducibilità

Metodo a quattro punte

per misura della resistività

(elimina effetto resistenza dei

contatti)

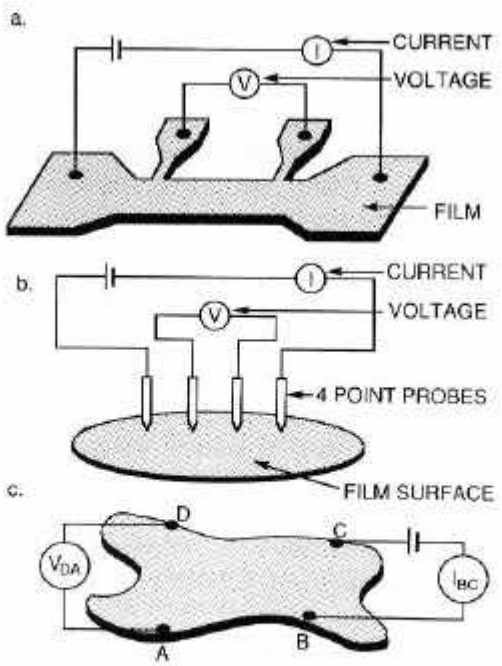


Figure 10-1. Techniques for measuring thin-film electrical resistance. (a) Four-terminal method for conducting stripes. Current is passed through outer terminals, and voltage is measured across inner terminals. (b) Four-point probe method for measuring sheet resistance. (c) Van der Pauw method for measuring resistivity of arbitrarily shaped film.

*Come la bassa dimensionalità (in una direzione) modifica **classicamente** la conduzione??*

Proprietà di trasporto (elettronico) in film sottili conduttori e semicond.

- Proprietà del film (esempio: porosità, reattività chimica superficiale, etc.)
- Effetti degli elettrodi (vedi MOS, ma anche MIM, SOS, MIS, etc.)
- Effetti di size:
  - scattering di elettroni all'interfaccia e in superficie
  - grain boundary effects (in materiali policristallini)

Da M. Ohring, The materials science of thin films (Academic, 1992)

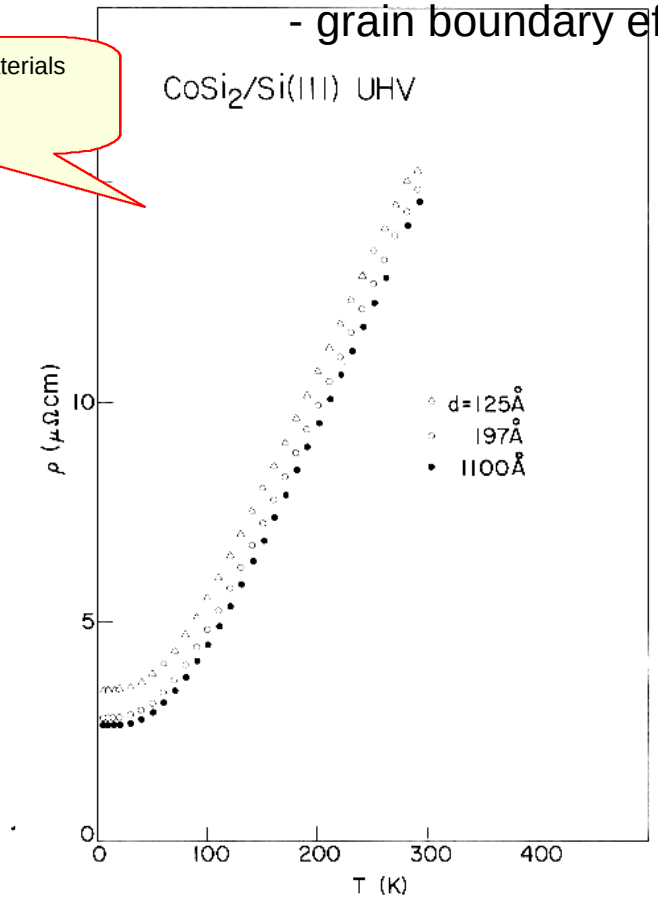


Figure 10-6. Temperature dependence of resistivity of $CoSi_2$ films. The 125-Å and 197-Å films are epitaxial. The 1100-Å film is polycrystalline. (From Ref. 10).

ρ vs T in film di $CoSi_2$ con diverso spessore: l'asintoto a T⟶0 mostra le caratteristiche di trasporto "intrinseche" del film (si può trascurare urti con fononi), che dipendono dallo spessore causa scattering alla superficie e all'interfaccia con il substrato. Inoltre la natura policristallina dei film contribuisce attraverso scattering (e altri effetti) a bordo grano.

Qui si trascurano gli effetti di confinamento quantico!!

Proprietà di trasporto (elettronico) in film sottili isolanti e semicond.

Table 10-2. Conduction Mechanisms in Insulators

Mechanism	J–$\mathcal{E}$ Characteristics		Experimentally Derivable Material Constants
1. Schottky Emission	$J_S = AT^2 \exp -\frac{q\Phi_B}{kT} \exp\left[\frac{1}{kT}\left(\frac{q^3\mathcal{E}}{4\pi\varepsilon_i}\right)^{1/2}\right]$	(10-21)	Φ_B
2. Tunneling	$J_T = \frac{q^2\mathcal{E}^2}{8\pi h\Phi_B} \exp -\left[\frac{8\pi(2m)^{1/2}}{3hq\mathcal{E}}(q\Phi_B)^{3/2}\right]$	(10-22)	
3. Space Charge Limited	$J_{SCL} = \frac{9\mu\varepsilon_i}{8}\frac{\mathcal{E}^2}{d}$	(10-23)	—
4. Ionic Conduction	$J_I = \frac{a\mathcal{E}}{kT} \exp -\frac{E_i}{kT}$	(10-24)	E_i
5. Intrinsic Conduction	$J_{in} = bT^{3/2} \exp -\frac{E_g}{2kT} \cdot \mathcal{E}$	(10-25)	E_g
6. Poole–Frenkel Emission	$J_{PF} = c\mathcal{E} \exp -\frac{E_i}{kT} \exp\left[\frac{1}{kT}\left(\frac{q^3\mathcal{E}}{\pi\varepsilon_i}\right)^{1/2}\right]$	(10-26)	E_i

a, b, c = constant.
ε_i = insulator dielectric constant.

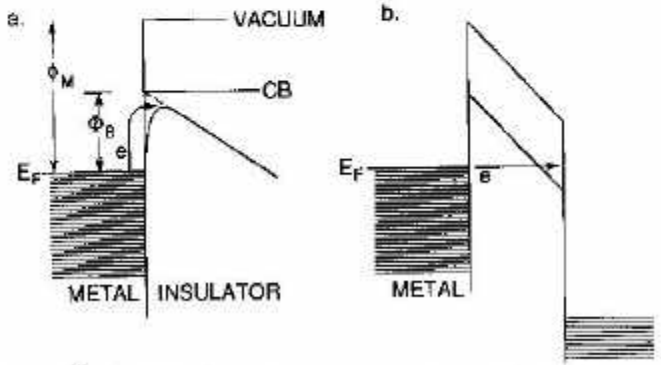


Figure 10-7. Barrier limited conduction mechanisms. (a) Schottky emission; (b) tunneling.

Processi di barriera (Schottky em., Tunnel) e processi di bulk (Cond. ionica, Poole-Frenkel,...)

Da M. Ohring, The materials science of thin films (Academic, 1992)

Qui si trascurano gli effetti di confinamento quantico!!

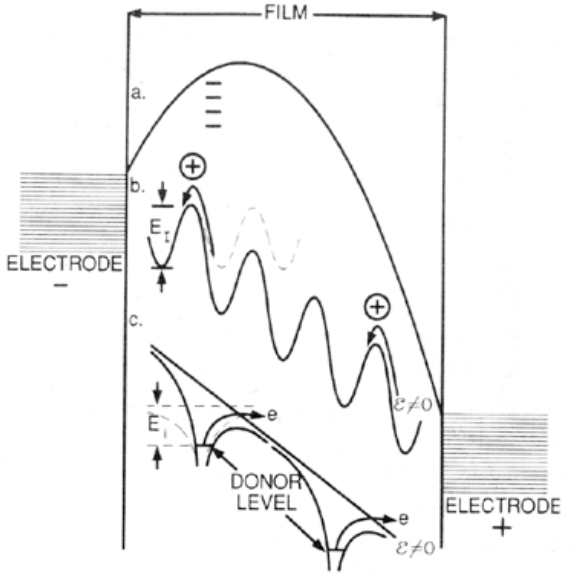


Figure 10-8. Bulk-limited conduction mechanisms. (Dotted lines refer to $\mathcal{E} = 0$) (a space-charge-limited; (b) ionic conduction of cations ⊕; (c) Poole–Frenkel.

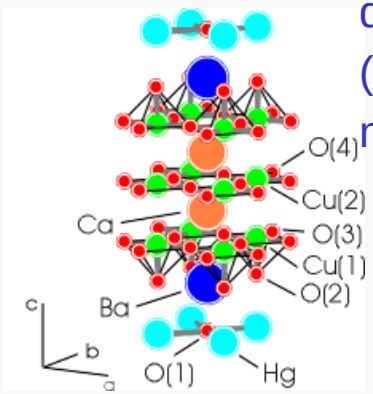
Considerazioni generali sulle proprietà di trasporto (classiche) in film sottili

- Processi legati alla natura chimico/strutturale del film (difetti, granularità…)
- Processi legati al rapporto superficie/volume (interfaccia, scattering in superficie…)

In generale: peggioramento delle caratteristiche
(isolanti per dielettrici, conduttrici per conduttori)

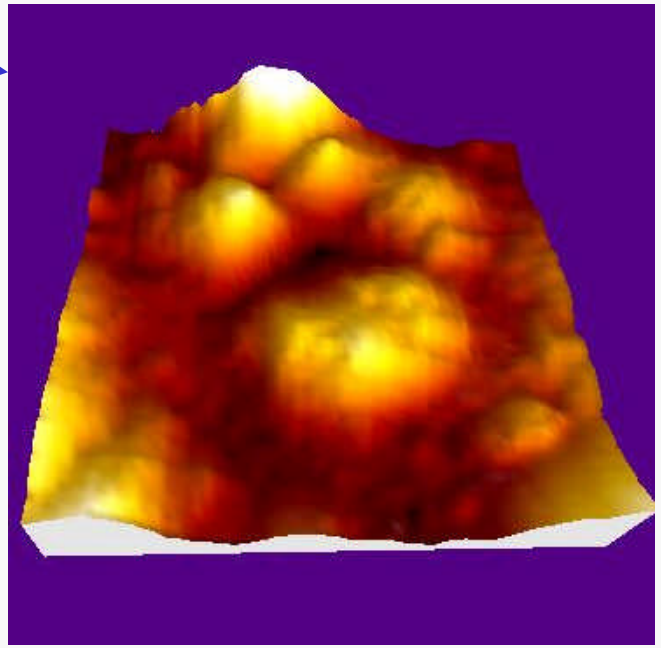
Eccezioni: materiali **policristallini** con struttura complessa

Esempio: superconduttori ceramici ad alta temperatura critica



AFM image of YBCO film deposited onto metal subs. (scan size approx 2x2 μm^2, max. height approx 180 nm)

YBCO ($YBa_2Cu_3O_{7-x}$)
T_c ~ 91 K (per x<0.5)



La conduzione su scala macroscopica implica tunneling fra diversi grani cristallini; la forma di film sottile permette crescita semi-epitassiale con bordi grano vicini e ben allineati