Scuola di Dottorato in Fisica Applicata “G. Galilei” - a.a. 2004/05

Topics in Nanotechnology – part 1

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Filling the gap between micro- and nanotechnology

6/4/2005 – 16-18 – room T1

Outlook

• What is *nanotechnology?*

• What are the *components* of nanotechnology?

• What are the main *driving forces* for development of nanotechnology

• What is the *present status* of technology?

• *Conventional* electronics:
  • Electron transport (Drude model);
  • Bipolar junctions (old-style technology);
  • Planar technology and MOS-FETs, DRAMs

• Some *limits and problems* in miniaturization and the need for new approaches

(Nano)technology

Technology: the ability to produce *small* (**nano**) systems **useful** for some application
i.e., the ability to manipulate matter in order to fabricate systems (or structures, or devices) with a size in the **sub-micrometer** range

Technology uses techniques, but **it is not just a technical application**: basic science is involved as well in designing new techniques and new structures with improved functionalities

(Nano)technology is strictly connected with basic science, but **it is not just investigation/interpretation** of processes in the nano-wrold

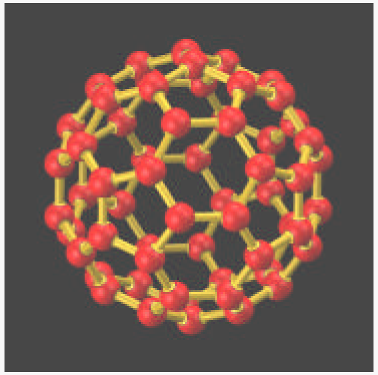
Nanotechnology is a "complex" (and rather vague) matter

[concepts from M.Wilson et al., Nanotechnology (Chapman&Hall, 2002)]

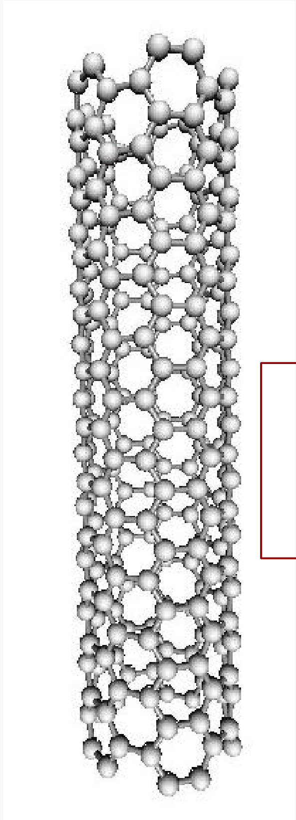
An example

BASIC SCIENCE

NANOTECHNOLOGY



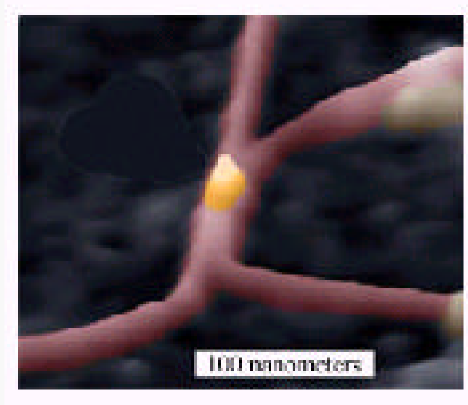
Fullerene (C_{60})



Single Wall
Carbon NanoTube

Mesoscopic systems (interesting for their physico-chemical properties

An artificial system made of CNT and gold nanoparticle intended to be a prototypal single-electron device



Components of nanotechnology

Nanotechnology shares topics with other disciplines,
but it **should not be confused** with:

-Chemistry, for the higher *control* of the involved processes;
-Materials science, for the specific interest in the small world;
-Physics, for the complexity of the systems under investigation;
-Engineering, for the specific interest in new systems
-Biophysics, (self assembly and replication) for the *artificial* systems

Nanotechnology is an "open" and strongly interdisciplinary field

Another example

Organic Light Emitting Diodes (OLEDs)

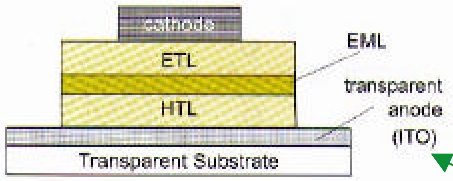
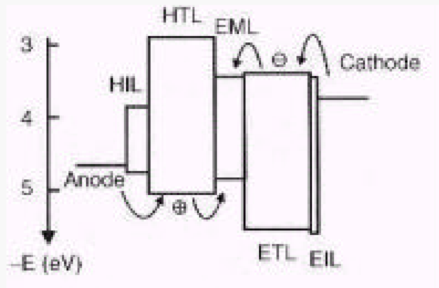


Figure 1: Schematic cross section of an organic light emitting device (OLED) showing the contacts, the electron transport layer (ETL), the light-emitting layer (EML) and hole transport layer (HTL). The total thickness of the organic layers is typically around 100 nm.

Engineering



Solid-state physics

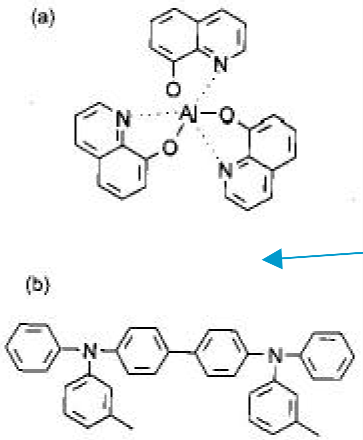


Figure 2: Chemical structures of
(a) Alq_3, an electron transport and green fluorescent emitting material and
(b) TPD, a hole transport material.

Chemistry +
Materials Science
(fabrication)

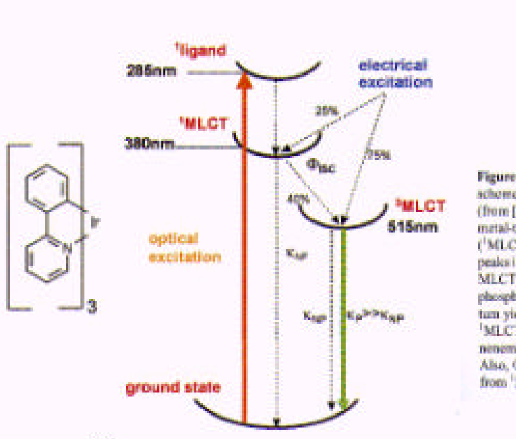


Figure 7: Chemical structure and energy level scheme for the metalorganic phosphor, $Ir(ppy)_3$ (from [38]). The ligand singlet state (^{1}ligand) and metal-to-ligand charge-transfer singlet state ($^1MLCT=S_1$) were determined by the absorption peaks in toluene solution (10^{-3} M). Also, the triplet MLCT state ($^3MLCT=T_1$) was estimated from the phosphorescence peak. κ_{NR}, κ_P, and κ_{NP} are quantum yields for nonemissive transitions from ^1MLCT intrinsic phosphorescent transitions, and nonemissive transitions from ^3MLCT, respectively. Also, Φ_{ISC} is the yield for intersystem crossing from ^1MLCT to ^3MLCT.

Molecular physics

An hystorical example of nanotechnology

Lycurgus Cup in Roman times

Dr. Juen-Kai Wang

The glass appears green in daylight (reflected light), but red when the light is transmitted from the inside of the vessel.

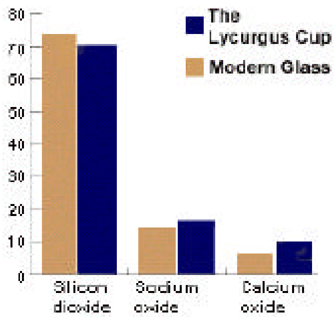
"Nanostructured" glass

The Lycurgus Cup, Roman (4th century AD), British Museum *(www.thebritishmuseum.ac.uk)*
F. E. Wagner et al., Nature ***407****, 691 (2000).*

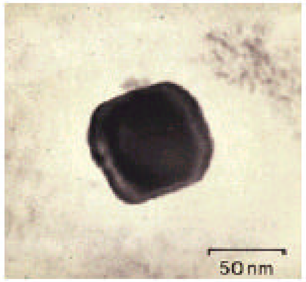
Optical properties of nanoparticles

Mysterious red color in Lycurgus Cup

Dr. Juen-Kai Wang



The same composition as modern glass



X-ray analysis: 70% Ag + 30% Au

These Ag-Au nanoparticles (~300 ppm) scatter the light, rather in the same way that fine particles in the atmosphere cause a 'red sky at night' effect. They cause the color effects shown by the Cup.

The Lycurgus Cup, Roman (4th century AD), British Museum (www.thebritishmuseum.ac.uk)

"New" functions (color effects) due to nanoparticles *intentionally created*

Gold Building Blocks

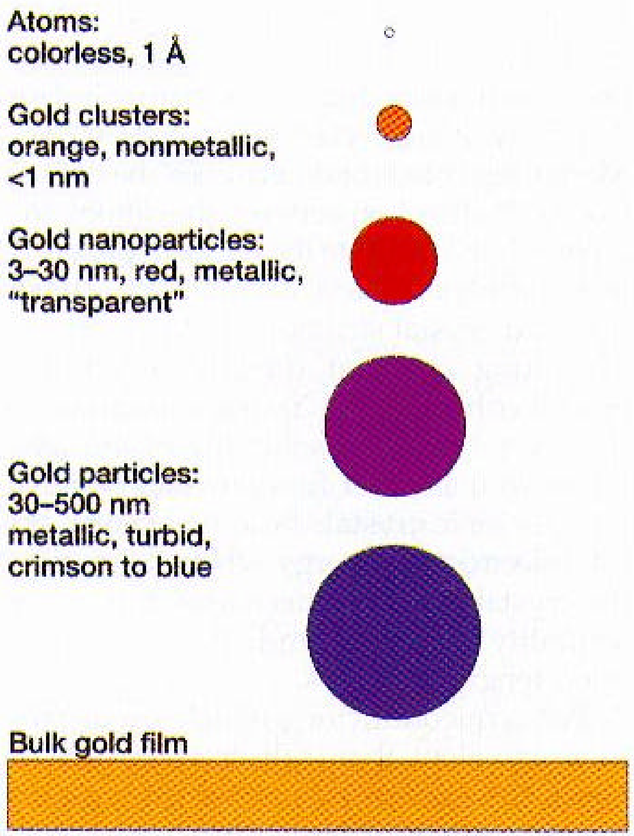


Figure 1. Gold building blocks, from the atomic to the mesoscopic, and their changing colors.

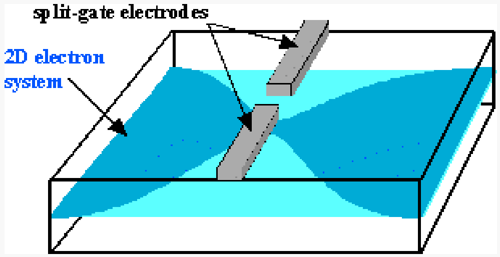
Our point of view

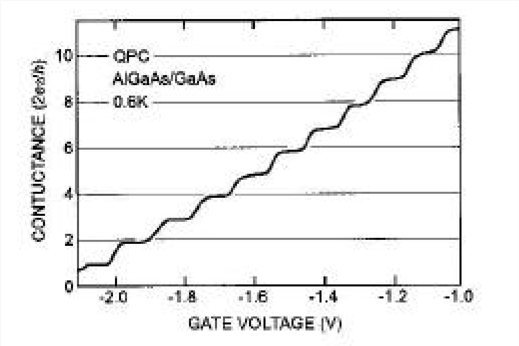
Selected topics of interest in (applied) physics:

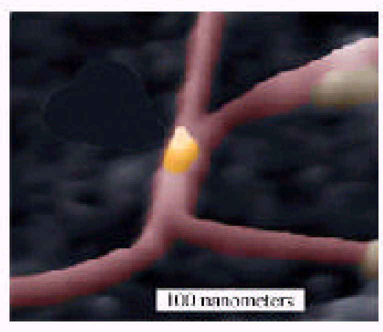
1. *Physical* methods for **fabrication** of nanostructures (i.e., evaporation, lithography, atom manipulation)

2. *Physical* **properties** of nanostructures (i.e., electron transport)

3. *Physical* tools for nanostructure **investigation** (i.e., probe microscopy)







There is plenty of room at the bottom…I

There's Plenty of Room at the Bottom

An Invitation to Enter a New Field of Physics

by Richard P. Feynman

This transcript of the classic talk that Richard Feynman gave on December 29th 1959 at the annual meeting of the American Physical Society at the California Institute of Technology (Caltech) was first published in the February 1960 issue of Caltech's *Engineering and Science*, which owns the copyright. It has been made available on the web at http://www.zyvex.com/nanotech/feynman.html with their kind permission.

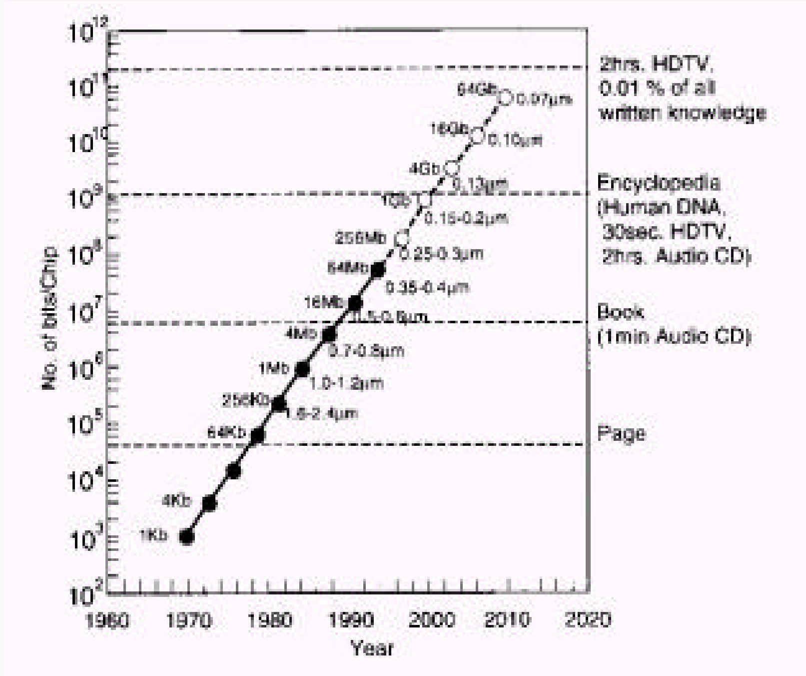
How do we write small?

Information on a small scale

Miniaturizing the computer

Miniaturization by evaporation

Miniaturization means increase of "power"

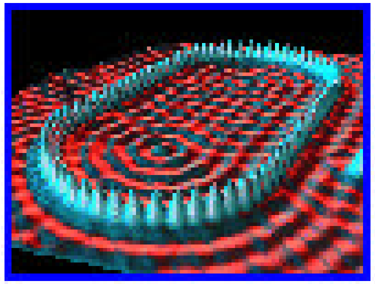


There is plenty of room at the bottom…II

Better electron microscopes

Atoms in a small world

Rearranging the atoms

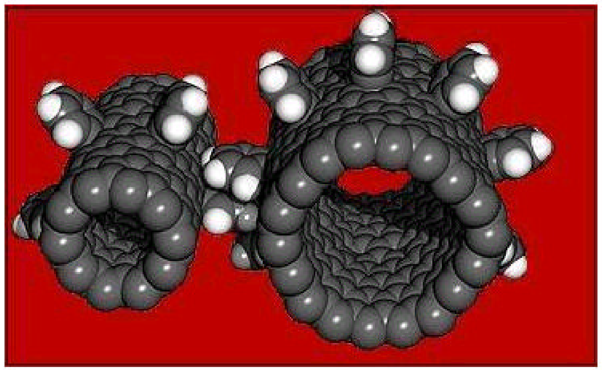


Title : Stadium Corral

Media : Iron on Copper (111)

IBM

Miniaturization means new (*quantized*) functionalities exploitable in novel applications



A representation of nanogears made from graphitetubes billionths of a meter wide. (Picture from the NanoGallery, see references)

4 • NANOTECHNOLOGY

'nanotechnology is the principle of atom manipulation atom by atom, through control of the structure of matter at the molecular level. It entails the ability to build molecular systems with atom-by-atom precision, yielding a variety of nanomachines.'

Eric Drexler (1990)

Nanomachines for, e.g., computation, drug dispensing, nanofluidics, …

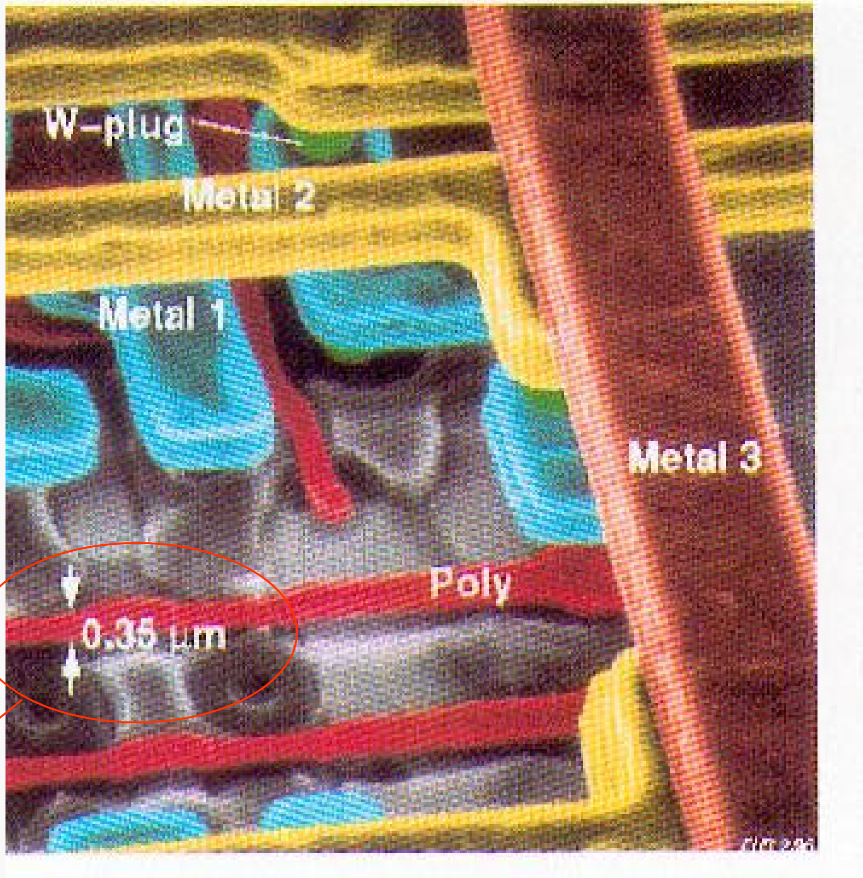
Manipulation and control of the matter at the single atom level

Driving forces for nanotechnology

Electronics devices:
they are typically (and *traditionally*) made of "small" structures

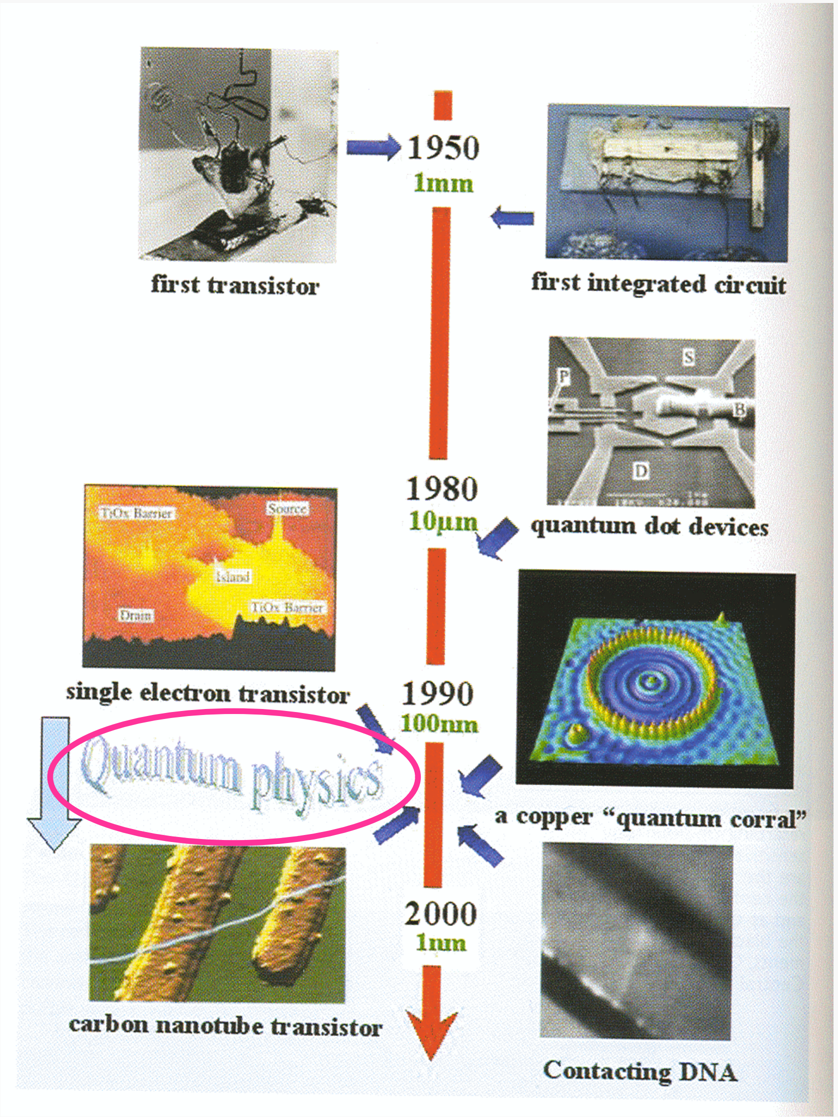
1. Thin films are deposited
2. A pattern is tranferred to the multilayered structure

Device components (resistors, capacitors, transistors, …) are so defined in an *integrated* structure



Feature size
(typ., fwhm of the smaller device features)

Progress in electronics (in the XX century)



Bipolar transistor

Planar (thin film) technology

Optical lithography

Very Large Scale Integration

Quantum confinement

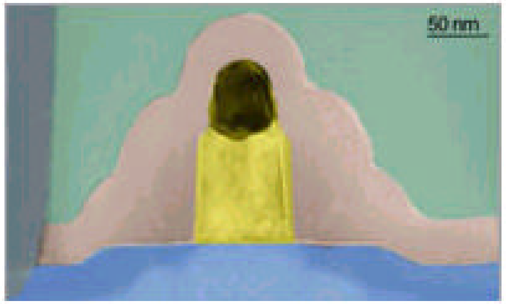
Alternative materials
and technologies

???

The present status of miniaturization

How many transistors can dance on the head of a chip only 66 millimeters square? Over 58 million, thanks to IBM's sophisticated process technology that builds them just 90 nanometers wide. Such superior technology developments turbo-charge the G5 processor to speeds of up to 2.5GHz.

To get electronics so small requires miniaturization breakthroughs, and IBM's dedication to basic scientific research makes these advances possible. For instance, the company began researching copper as an interconnect method over 25 years ago, but the technique wasn't practical until just recently.



One in 58 Million. A transistor just 90nm wide (yellow) on substrate of SOI (blue) with copper interconnects (gray). Layers of nitride (brown) and oxide (green) insulate it from its brethren. Magnified 146,000 times.

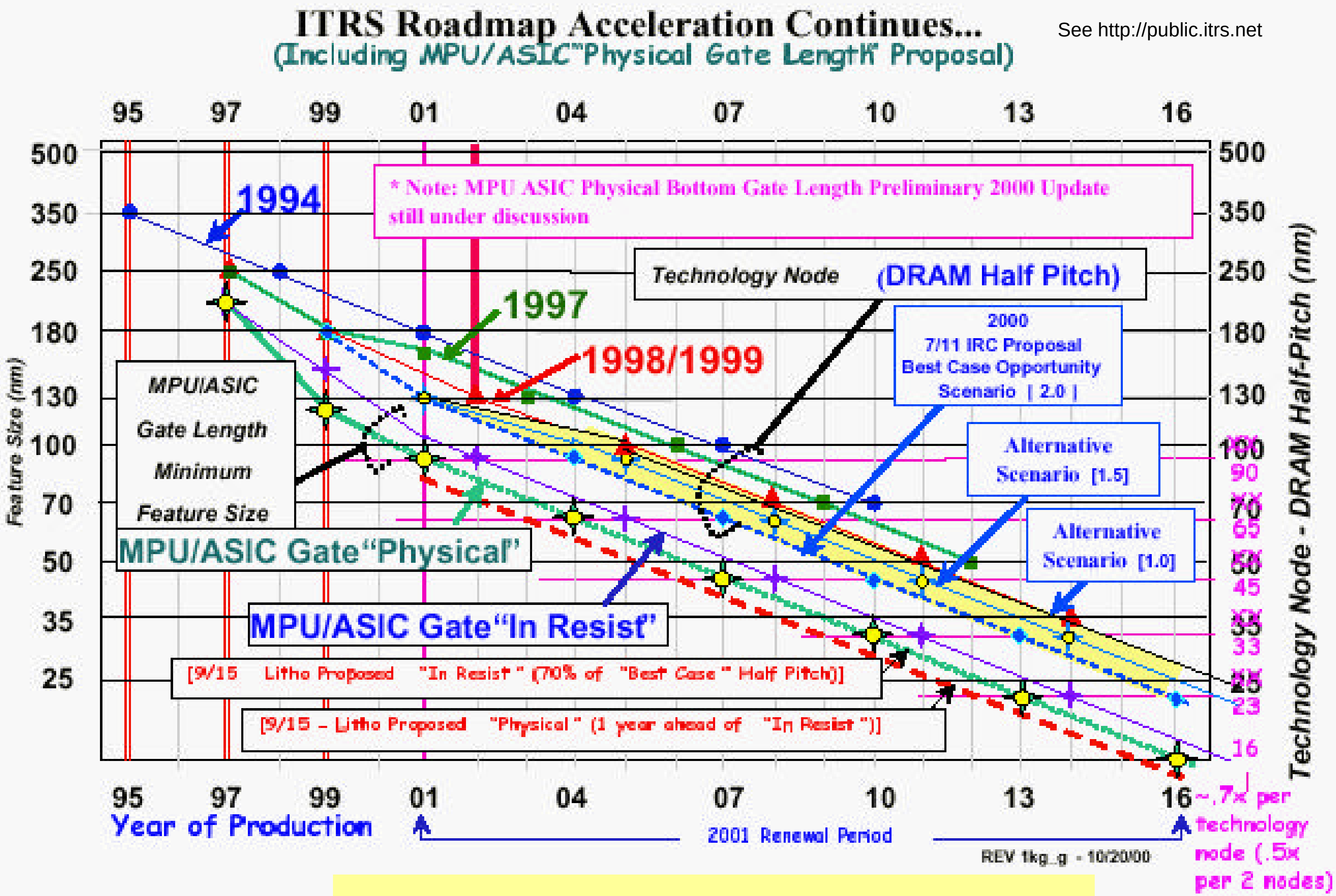
So Small

Transistors on the PowerPC G5 hold a charge to let the system make logic decisions based on whether the transistor is on or off. Using a 90nm process for even greater performance, IBM builds these devices just .00000009 meters wide on a layer of silicon on insulator. The 58 million transistors themselves are connected by over 400 meters of copper wire that's less than 1/1000th the width of a strand of your hair. Tiny paths mean less time to complete a sequence, since the

http://www.apple.com

Feature size slightly below 100 nm (nanotechnology?)

The “Moore’s law”



“Miniaturization” increase by a factor 3-4 in a 3-4 year period (still true?)

Technical and fundamental problems

- In order to maintain the progress of Moore's Law, the 2001 ITRS envisions **more aggressive scaling than projected in prior roadmaps**. For example, dynamic random access memory chips will feature critical dimensions of 90 nanometers in 2004, which is both smaller and sooner than the 100 nanometers projected for 2005 in the roadmap published just two years ago. Similarly, microprocessor transistor gate lengths -- a critical dimension that affects the processor's speed -- will be just 25 nanometers in 2007, six years sooner than expected in the 1999 version of the roadmap. (Note: a nanometer is one-billionth of a meter. A human hair is 100,000 nanometers in width, and a red blood cell is 5,000 nanometers in width.)
- **We are beginning to reach the fundamental limits of the materials used in the planar CMOS process**, the process that has been the basis for the semiconductor industry for the past 30 years. Further improvements in the planar CMOS process can continue for the next five to ten years by introducing new materials into the basic CMOS structure. However as the ITRS looks forward 10-15 years, it becomes evident that even with the introduction of new materials, most of the known technological capabilities of the CMOS device structure will approach or have reached their limits. In order to continue to drive information technology advances, it becomes necessary to investigate new devices that may provide a more cost-effective alternative to planar CMOS in this timeframe.

Da www.sia-online.org

The rate of increase in miniaturization has been growing fast
In information tchnology

Main motivations:
- Increase of "power" (computing efficiency, information storage, time response, …)
- Decrease of power consumption, usually associated with miniaturization
- Commercial reasons (a huge market!)

Technical limitations: lack of control in the manipulation, limits of the materials

Fundamental limitations: in the **techniques** (e.g., optical diffraction in lithography), in the **system operation** (e.g., *quantum* behavior)

Need for novel approaches

Basics of *conventional* electronics I

Diffusive electron transport (Drude)

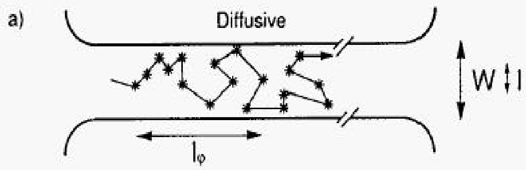


Figure 10.4: Electron trajectories characteristic of the diffusive ($\ell < W, L$), quasi-ballistic ($W < \ell < L$), and ballistic ($W, L < \ell$) transport regimes, for the case of specular boundary scattering. Boundary scattering and internal impurity scattering (asterisks) are of equal importance in the quasi-ballistic regime. A nonzero resistance in the ballistic regime results from backscattering at the connection between the narrow channel and the wide 2DEG regions. Taken from H. Van Houten et al. in "Physics and Technology of Submicron Structures" (H. Heinrich, G. Bauer and F. Kuchar, eds.) Springer, Berlin, 1988.

Diffusive means dissipative (resistance)

Classical interpretation (Drude):
Collisions betwen electrons and lattice ions lead to a friction force (and electrons do have thermal distribution of speed)
Quantum interpretation:
Collisions are replaced by loss of translational invariance in the electron wavefunctions (and the Fermi velocity must be considered)

Drift (limit) velocity:

$v_d = \tau \, eE/m^*$

but $\mathbf{J} = n\, e\, \mathbf{v_d}$

hence: $\sigma = n\, e^2 \tau / m^*$

"Microscopic" Ohm's law:

$\mathbf{J} = \sigma \mathbf{E}$

$\sigma = n\, e^2 \tau / m^*$

τ : time interval between collisions

m* : effective mass of the charge carriers

Transport in metallic thin films

Thin film can be considered as a *one-dimensional* example of nanotechnological system

Da M. Ohring, The materials science of thin films (Academic, 1992)

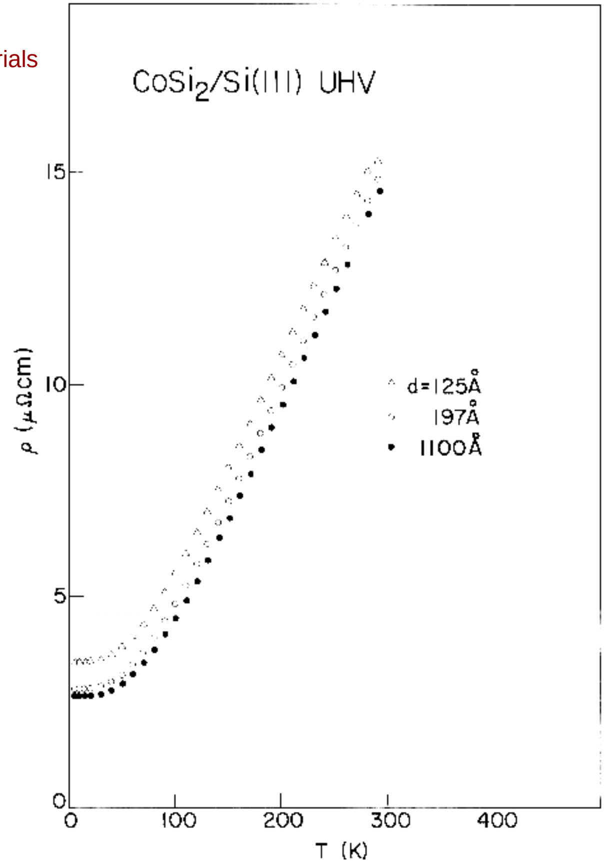


Figure 10-6. Temperature dependence of resistivity of $CoSi_2$ films. The 125-Å and 197-Å films are epitaxial. The 1100-Å film is polycrystalline. (From Ref. 10).

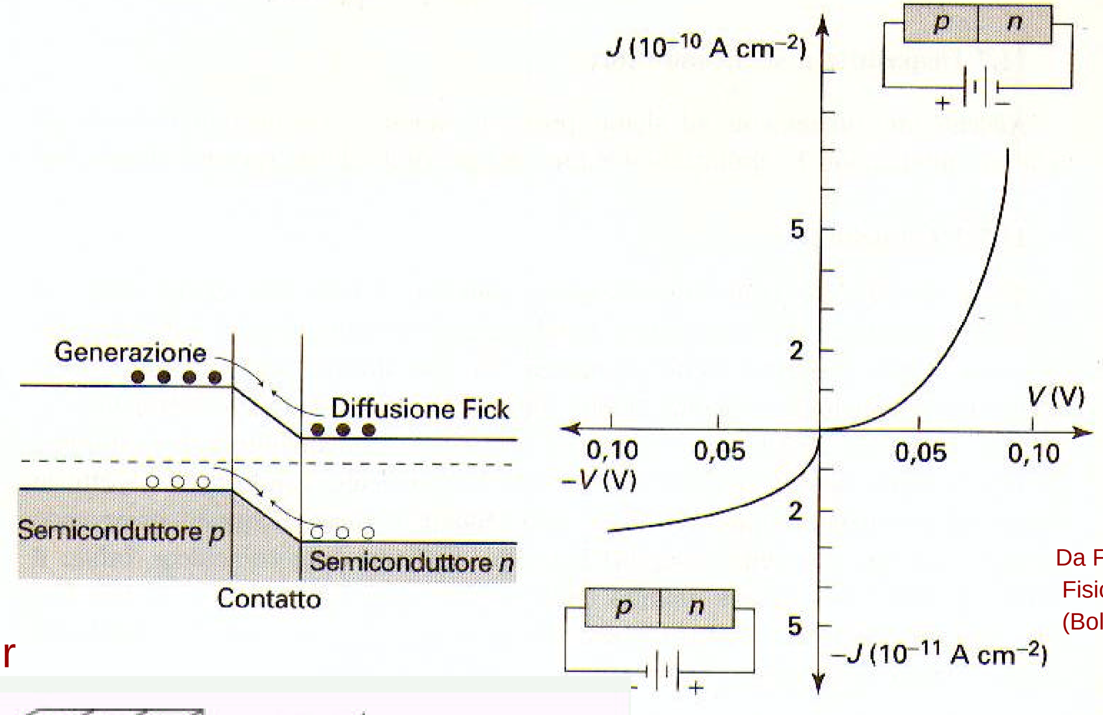
Neglecting any quantum-confinement effect

Resistivity tends to increase with decreasing film thickness due to the increased role of the electron collisions at the film interface

Interface gets important in ruling the system behavior

Basics of *conventional* electronics II

Bipolar junction



Da F.Bassani, U.M. Grassano,
Fisica dello Stato Solido
(Bollati Boringhieri, 2000)

Bipolar transistor

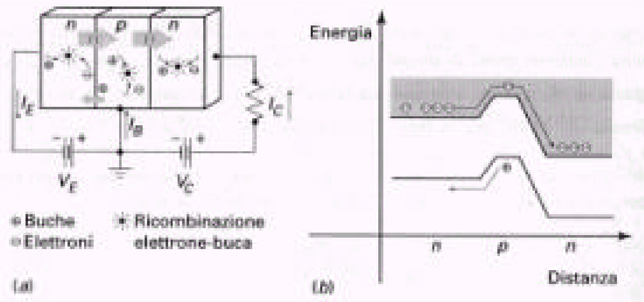


Figura 11.16
Transistor n−p−n, con i relativi simboli per indicare la corrente di emettitore (I_E), di collettore (I_C), e la corrente di base (I_B). (a) Indicazione degli stati di polarizzazione e dei flussi di corrente (buche ed elettroni). (b) Posizionamento delle bande in presenza di un campo (diretto per la giunzione n − p).

A current (e.g., BE) is used to control a current flow (e.g., CE)

Power consumption issues!

Old-style technology

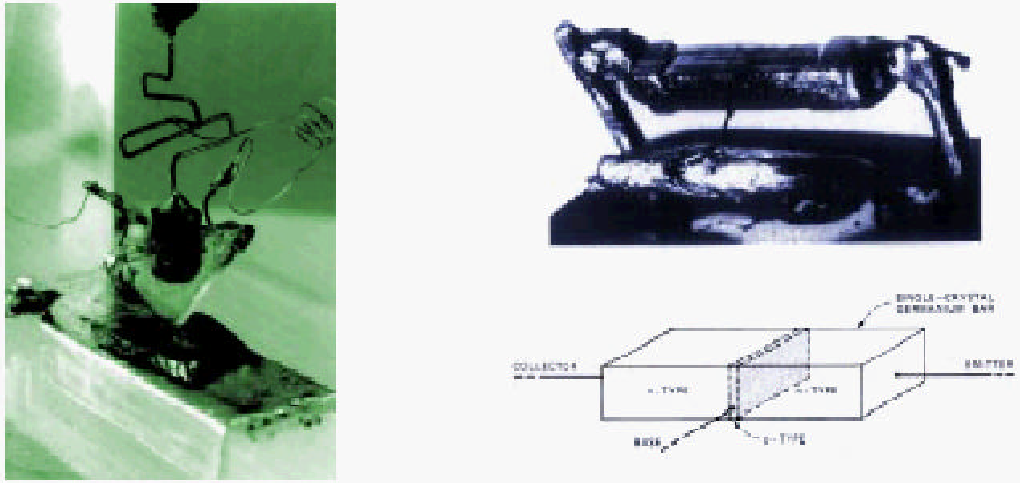
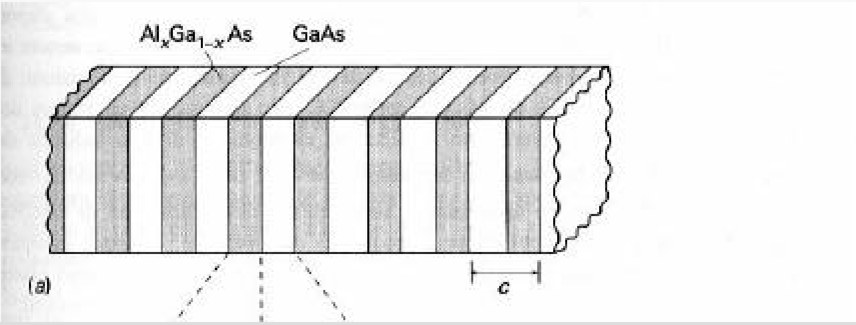


Figure 1 – The first transistors: (a) the point contact transistor of Brattain and Bardeen, 1947 (left); (b) the junction transistor of Shockley, Morgan, Sparks, and Teal, 1950 (right).

“Linear” technology did not allow for miniaturization

Basics of *conventional* electronics III

Planar technology (thin film multilayers of different materials)



Semiconductor heterostructures

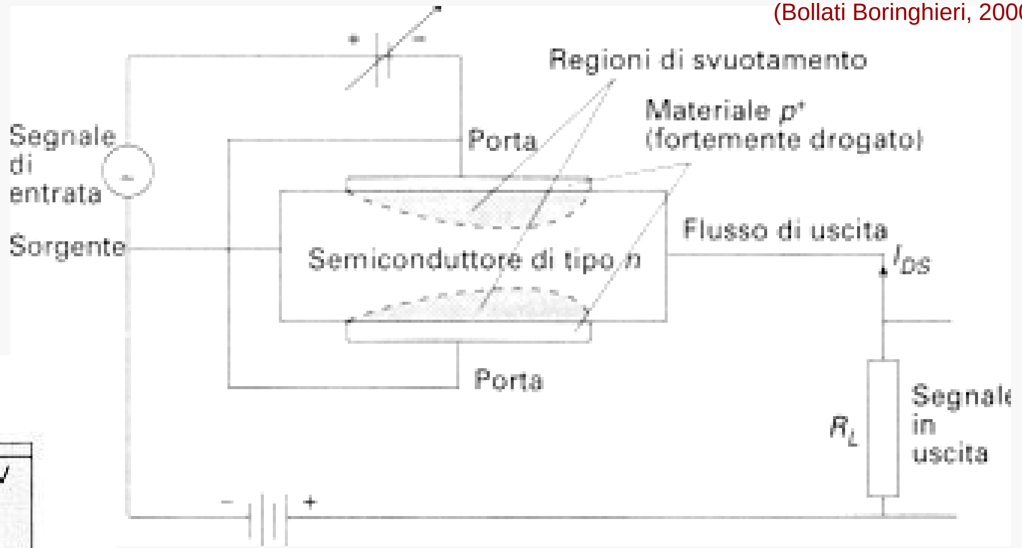
Dielectric films

Careful engineering of the material properties achieved by (one-dimensional) control at the few atomic layer level

The Field-Effect Transistor

Da F.Bassani, U.M. Grassano,
Fisica dello Stato Solido
(Bollati Boringhieri, 2000)

Basic concept of a Field-Effect Transistor (FET)



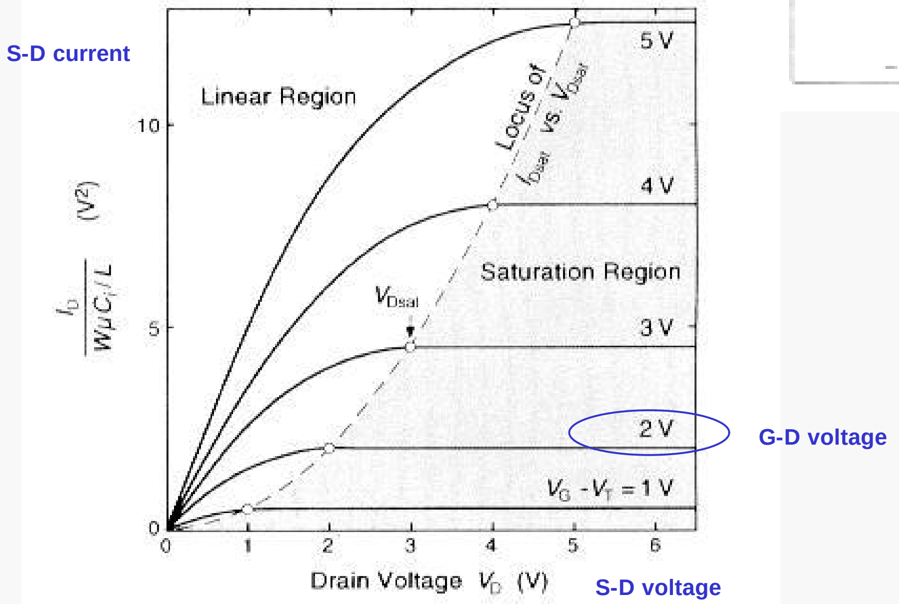


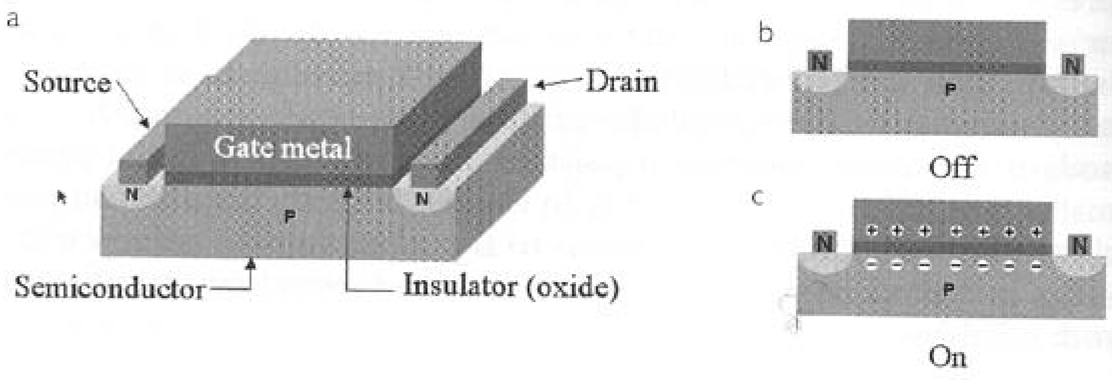
Figure 9: Idealized *I*-*V* curves of a MOSFET. The dashed line indicates the locus of I_{Dsat} vs. V_{dsat} [6].

The gate voltage is used to control the source-drain current

The MOS-FET I

Planar (thin film) technology is compatible with MOS-FET architectures

a) A schematic diagram of a MOSFET showing its switching operation,
b) with no voltage applied to the gate: OFF and
c) with a positive voltage applied to the gate: ON.



Key points:

- Metal-Oxide-Semiconductor (MOS) multilayer
- Thin dielectric layer (E=V/d!!)
- Lateral definition of the structure
- Large scale integration possible

Sub-micron (conventional) MOS-FET

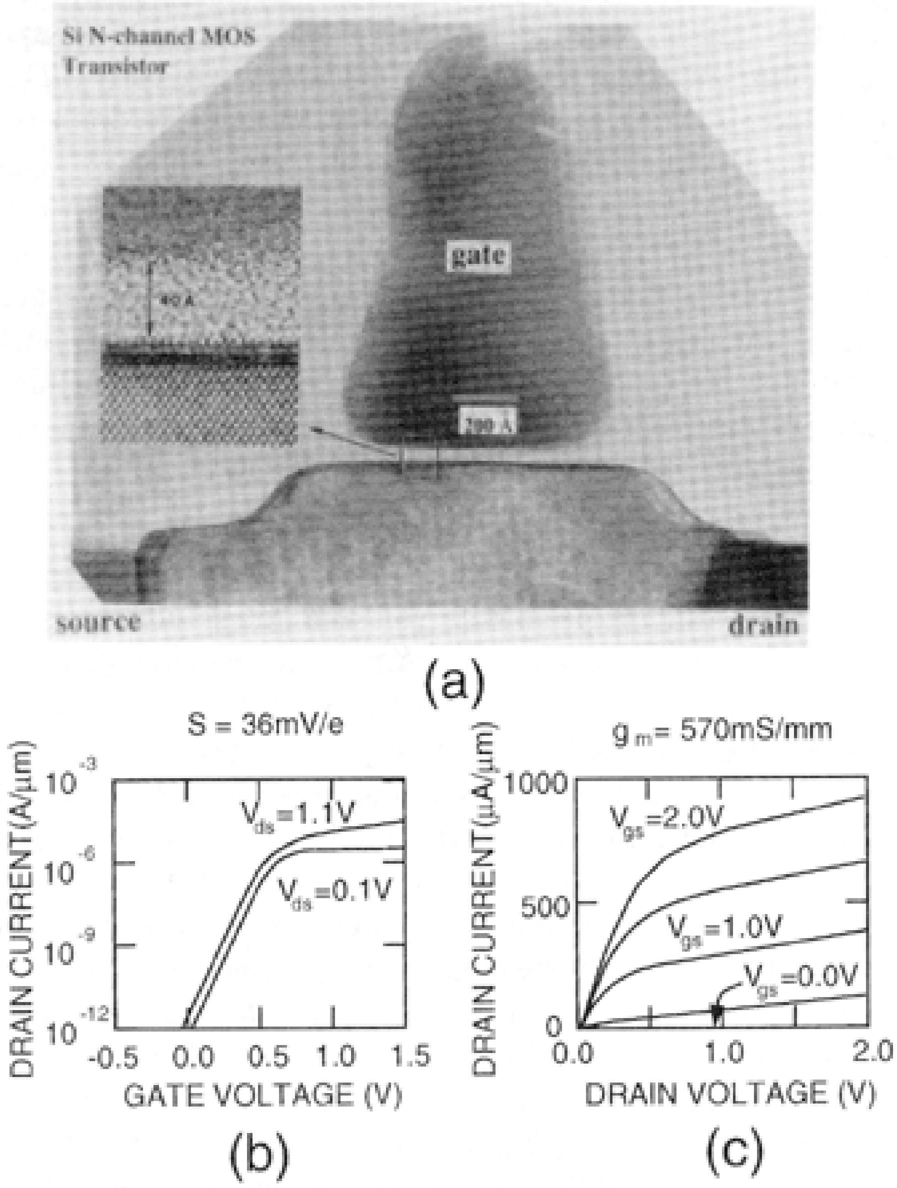


FIGURE 6. (a) A high-resolution transmission electron micrograph of a cross-section of an N-MOSFET with a gate length of 0.13 μm adapted from[27] and through the courtesy of Y. Kim. The channel is less than 400 atoms long. The inset shows a lattice image of the channel region of this device. (b) and (c) represent the measured subthreshold and drain characteristics found at room temperature for an N-MOS transistor like that shown in (a). From these measurement it can be inferred that the transconductance is approximately 570 μS/μm, and the subthreshold slope, $S = 36\ mV$ per e-fold change in I_D or $84 mV$/decade, and the threshold voltage is $V_t = 0.45\ V$.

Da G. Timp, Nanotechnology
(Springer-Verlag, 1999)

The MOS-FET II

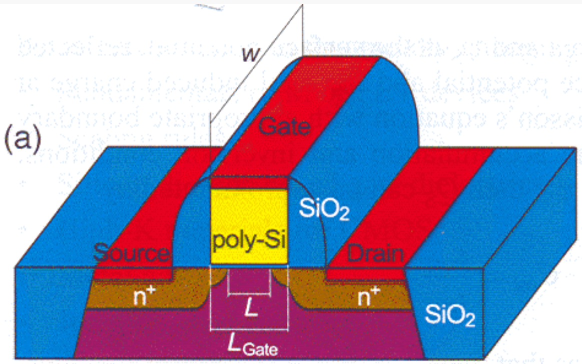
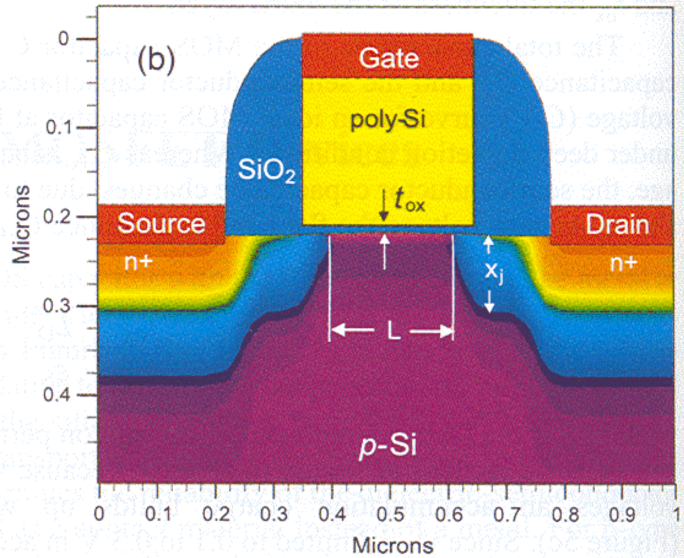


Figure 7:
(a) MOSFET device structure with the terminals, source, gate and drain. L_{Gate} denotes the (printed) gate length, L the channel length or physical gate length and w the gate width. The transistors are isolated with SiO_2 trenches on each side. The gate contact is isolated from source and drain with SiO_2 spacers on each side of the poly-silicon gate contact.
(b) Net doping profiles on a micrometer length and depth scale for a transistor with a gate length $L \cong 0.2$ μm and a gate oxide thickness t_{ox} as calculated with a device simulator (Silvaco). The colours reflect the net dopant concentrations in the Si, ranging from $\approx 10^{17}$ B cm^{-3} in the p-Si to $\approx 10^{20}$ As cm^{-3} near the source/drain silicide contacts. The depth of the n^+/p-junction at the extensions, indicated with x_j, is much shallower than the junction depth below the source and drain contacts (at the blue/dark red boundary).



Modulation doping for the semiconductor on a small scale

The MOS-FET III

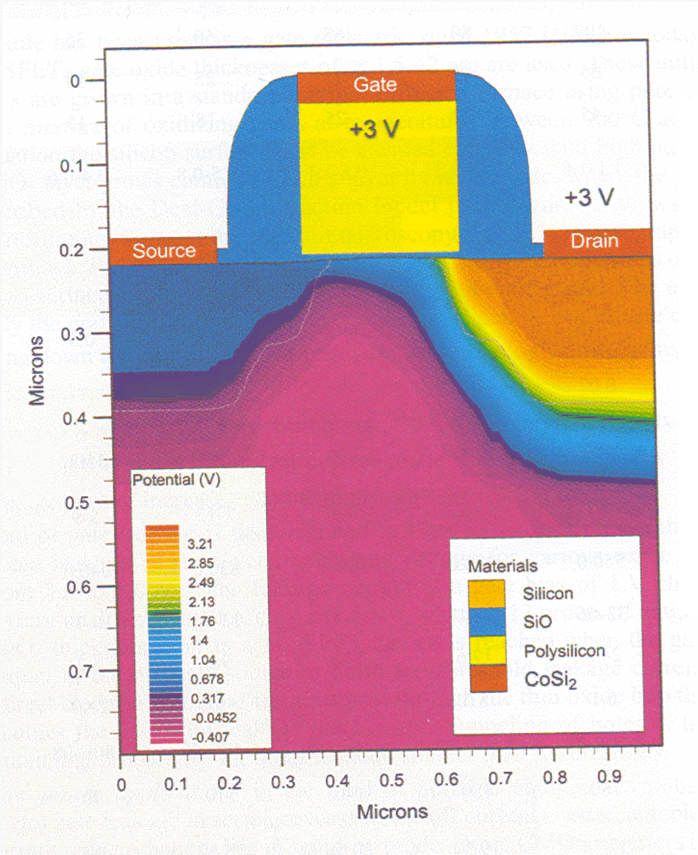


Figure 10: Simulated potential distribution of a 0.2 μm MOSFET with $V_G = 3$ V and $V_D = 3$ V. Near the drain region the potential lines are strongly affected by the drain voltage. The thin solid line indicates the n+/p-junctions.

Relatively large field gradients in small regions

Need to accurately control the material at the nanometer scale

⇩

Limits in miniaturization

Tiny MOS capacitor

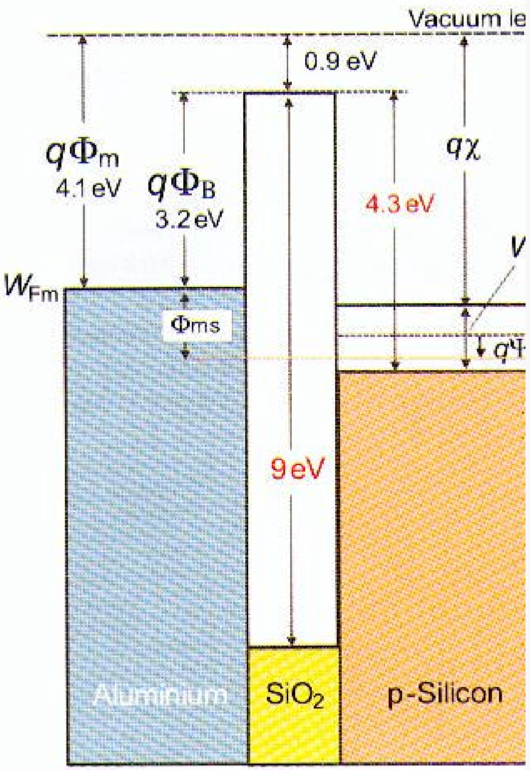


Figure 4: Energy-band diagram of the thı components of a real MOS capacitor, con ing of an Al contact, silicon dioxide and p- silicon. $q\Phi_m$ denotes the work function o metal, $q\Phi_{ms}$ the workfunction difference c versus p-Si, χ the electron affinity of the con, W_g the band energy, W_c the conducti band, W_v the valence band of silicon, $q\Psi_F$ difference between the intrinsic Fermi lev and the Fermi level W_F [5].

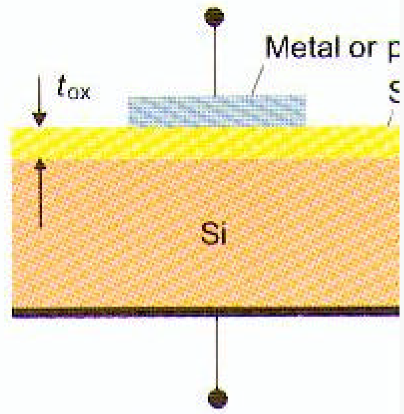


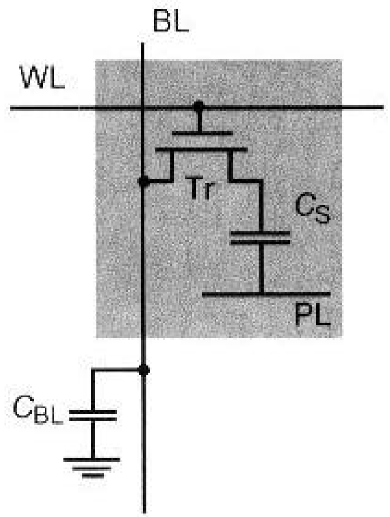
Figure 3: Schematic structur of a MOS capacitor.

MOS capacitor (fabricated by planar technology + large integration lithography) can be used in memories (information is kept in the capacitor)

Da R. Waser Ed., Nanoelectronics and information technology (Wiley-VCH, 2003)

Random-Access Memories I

DRAM



Flash NVRAM

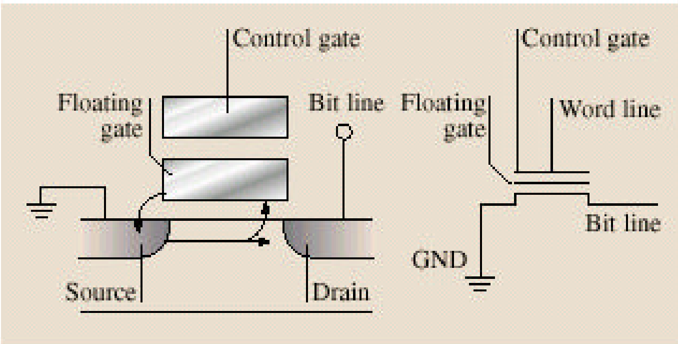


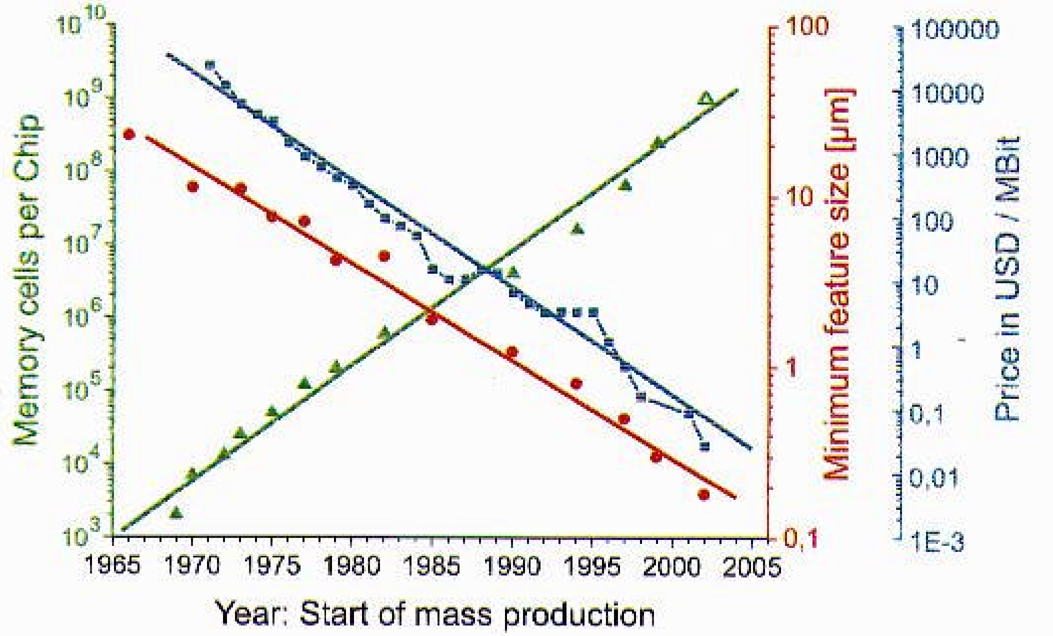
Fig. 30.9 Schematics diagram of a typical Flash Memory cell

MOS capacitors are basic components of RAMs

Flash Memory

Flash Memory, the most common non-volatile, programmable memory device, uses rows and columns of interconnects that address each data cell. At the intersection of these are two transistors, which comprise the Flash Memory cell, as shown in Fig. 30.9. Each cell is addressed by a network of interconnects, where the common connection to the transistor gates is called the word line and the common connection to the drain is called the bit line. Every cell in the memory array can be accessed by activating a unique combination of these lines. Here, the floating gate is linked to a word line via a second gate that serves as a control gate. The floating gate potential is altered by Fowler–Nordheim tunneling of electrons, an effect that takes place when the applied bias needed for switching is larger than the work function of the relevant electrode. The electrons arrive from the column, or bit line, and enter the floating gate from which they drain to the ground. A cell sensor monitors the flow of electrons through the gate. A value of 1 is assigned when the current is greater than a given threshold value, and 0 if it is below that value. Approximately 30,000 electrons are stored in the gate to make a 1 and 5,000 for a 0. The memory of the device derives from the very long storage time (tens of years) of the tunneling electrons in the gate capacitor. For the data to have a lifetime of ten years, the electrons can leak at a rate of no more than five a day. Flash memory can only be rewritten a limited number of times (10^{5-6}), as electrons get permanently trapped in the gate over time, impairing device efficiency. Memory devices using this technology are SmartMedia, Com-

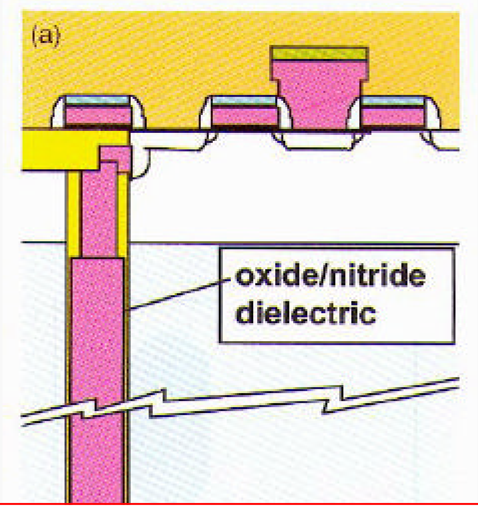
Random-Access Memories II



Strong technological (and economical) expectations for RAM miniaturization

ITRS Technology Nodes and Chip Capabilities[2]				
	2001	**2005**	**2010**	**2016**
DRAM Half-Pitch (nanometers)	130	80	45	22
DRAM Memory Size (mega or gigabits)	512M	2G	8G	64G
DRAM Cost/Bit (micro-cents)	7.7	1.9	0.34	0.042
Microprocessor Physical Gate Length (nanometers)	65	32	18	9
Microprocessor Speeds (MHz)	1,684	5,173	11,511	28,751

Sophisticated architectures



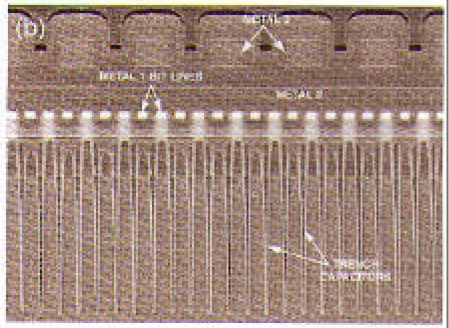


Figure 3: Example of a 3-D capacitor: (cross section) deep trench with oxide/nitride dielectric ($\varepsilon_r \approx 7$).
(a) Schematic, from [8];
(b) Scanning electron micrograph for Toshiba/Infineon 64 Mb chip. The design is similar in … 1 Gb chips with much higher aspect … / depth).

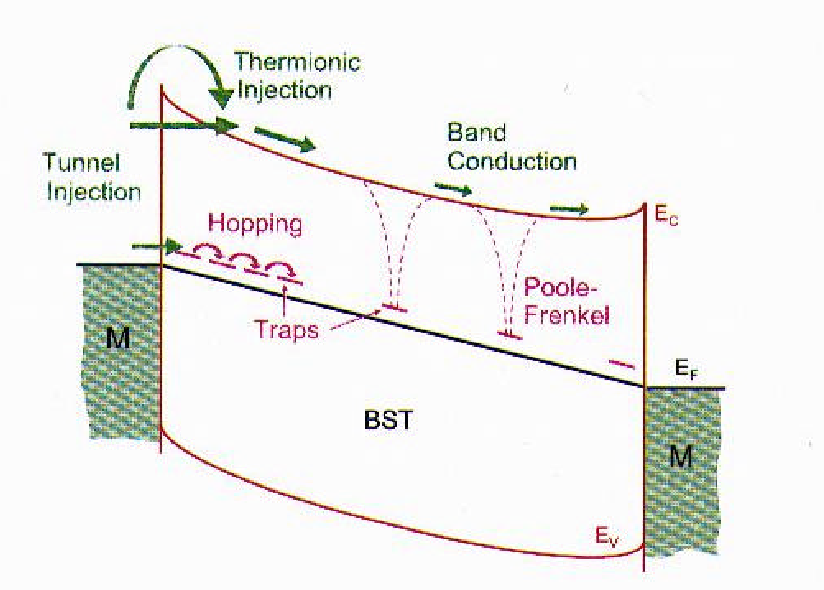
The value of the cell capacitance, C_S, varies only slowly with DRAM generation due to the same trends for the cell charge, Q_S, and the operating voltage, V_{DD}. For the 256 Mb chip, C_S is approx. 25 fF. The geometrical dimensions can be approximated very well by using the equation for the parallel plate capacitor:

$$C_S = \varepsilon_0 \varepsilon_r \frac{A_S}{t_{phys}} = \varepsilon_0 \varepsilon_{r,SiO_2} \frac{A_S}{t_{eq}} \quad \text{with } t_{eq} = \frac{\varepsilon_{r,SiO_2}}{\varepsilon_r} t_{phys} \text{ and } \varepsilon_{r,SiO_2} = 3.9. \qquad (1)$$

A_S is the total area of the capacitor, (defined by the surface area of the bottom electrode), t_{phys} is the physical thickness of the dielectric, and ε_r its relative permittivity, while ε_0 is that of vacuum. Eq. (1) also defines the equivalent dielectric thickness, t_{eq}, with respect to the relative permittivity of SiO_2, $\varepsilon_{r,SiO2} = 3.9$, as this dielectric was used at the beginning of DRAM history. With higher integration density, it was replaced by a mixture of Si oxide and nitride layers (ε_{r,SiN_x} approx. 11) with higher effective dielectric constant, the so-called ON dielectric. Starting with the 4 Mb generation, the required capacitor area, A_S, was too large for the cell area, A_{CA}, and the cell capacitance could not be achieved with a planar geometry. Consequently, the third dimension had to be used in the form of trenches (see Figure 3) and later also of posts in a stacked geometry (see Figure 4).

Classical behavior:
ultra low capacity involved
(C~S/d!!)

Limits of the dielectric materials



Dielectric behavior degrades when thickness is decreased

3 Challenges for Gb DRAM Capacitors

Entering the Gb era, the capacitor of the DRAM cell in the conventional design is approaching its limits: (i) The thickness of the (Si) oxide/nitride (ON) compound layer allows no further thinning beyond approx. 5 nm because of unacceptably high tunneling leakage currents (see Sect. 5.2) reducing the stored capacitor charge to too low values, and (ii) the 3-D geometry is already very complicated and, hence, rather expensive due to the high number of processing steps. Some examples of very advanced 3-D structures are shown in Figure 3 (trench capacitor) and Figure 4 (stacked capacitor). Both have been produced with the 250 nm technology, i.e. the minimum feature size, F, was 250 nm, which was used when this generation was introduced into the market. The DRAM cell area, A_{CA}, was approx. $12\,F^2 = 0.75\ \mu m^2$ and the equivalent thickness, $t_{eq} = 5$ nm (see Eq. (1)), which corresponds to a physically thicker layer using ON dielectrics [9]. The challenges of the capacitor for future Gb DRAM generations will be demonstrated with the help of a detailed description of Figure 3 and Figure 4. Some important characteristic numbers for these capacitors will be summarized in Table 1 together with the respective ones for higher permittivity materials such as Ta_2O_5 ($\varepsilon_r \approx 22$) or $(Ba,Sr)TiO_3$ (BST) ($\varepsilon_r = 200$).

The most impressive feature of the trench capacitors shown in Figure 3b is their depth, more than 7 µm with 250 nm width at the top resulting in an aspect ratio (i.e. depth/width) of near 30. Thus, the necessary capacitor area, $A_S = 5.1\ \mu m^2$ corresponding to a capacitance of 35 fF, can be supplied. The projected area of the trench capacitor in the cell area is only $2\,F^2 = 0.125\ \mu m^2$ or 16 % of A_{CA} (see Figure 5a). The reason for this small fraction can be realized from the schematic representation of a trench cell in Figure 3a. The cell area has to be shared with the select transistor and the local wiring, the capacitor is in an offset position similar to the planar capacitors in early DRAM generations.

Conclusions

Filling the gap between micro- and nanotechnology has to face:
-Inherent limitations in scaling down the feature size;
-Material limitations due to the small size (ultra thin films);
-(Fundamental problems in the fabrication process)
-(Fundamental issues associated with quantum confinement)

New approaches are required for fabrication

New architectures are required for the device operation

New diagnostics tools are needed

New functions can be achieved